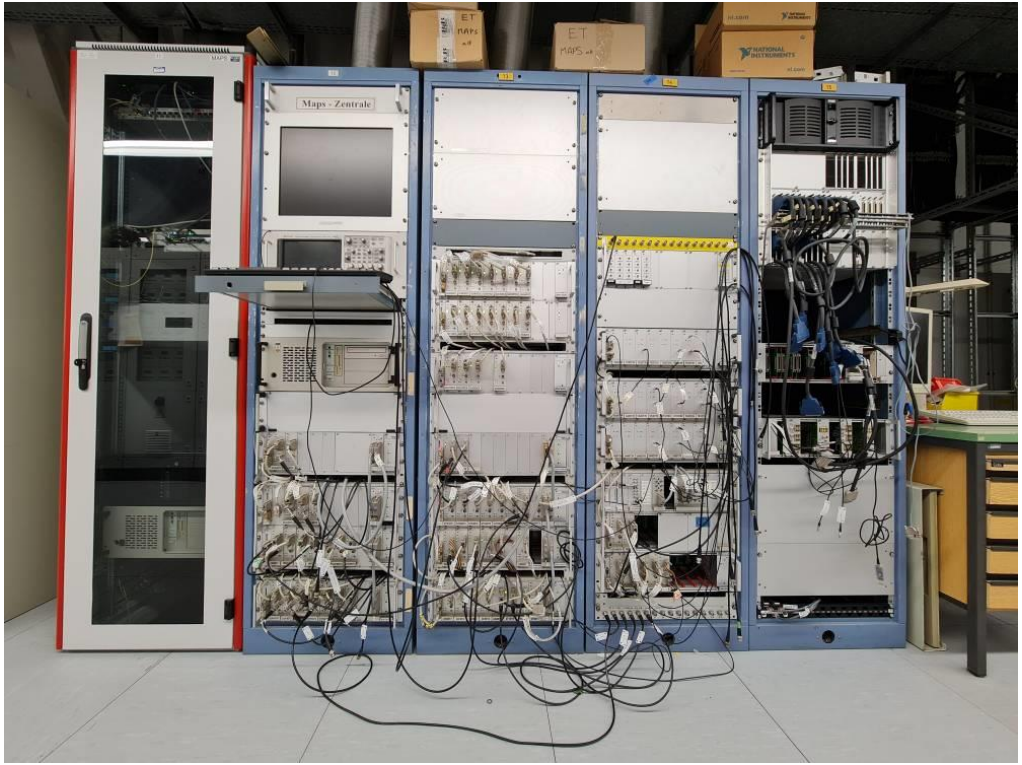
MAPS

MAPS - The Macro Pulse Selector @ UNILAC 2022

What is MAPS:

- Data Acquisition and display of UNILAC transformer data including gate pulses.
- Provides separate signals for SVÜ
- Part of the BTM system



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Project idea:

- Total renovation of the aged MAPS system, independed of FCC
- Replacement of all old DAQ hard- and software (x86 CPU on MS-DOS, Borland C)
- All signals will be digitized in parallel
- For commissioning: system signals will be splitted for parallel usage of old and new MAPS (only signals, not pre-amp power and I/O settings)
- The SVÜ will not be touched. We need to make sure, that the pre-amp is always powered. SVÜ signals will be converted into TTL pulses and offered to ACO.
- **A first prototype with readout of a few UNILAC transformers will be presented in the next beam time January 2022 -> NOT POSSIBLE**

Project objective at risk:

- Complex adaptor box not ready(e.g. missing components, order stop, delivery time)
- Lack of man power (parallel workload for beam operation and Hitrap, retirement)
- LSA not yet ready at UNILAC

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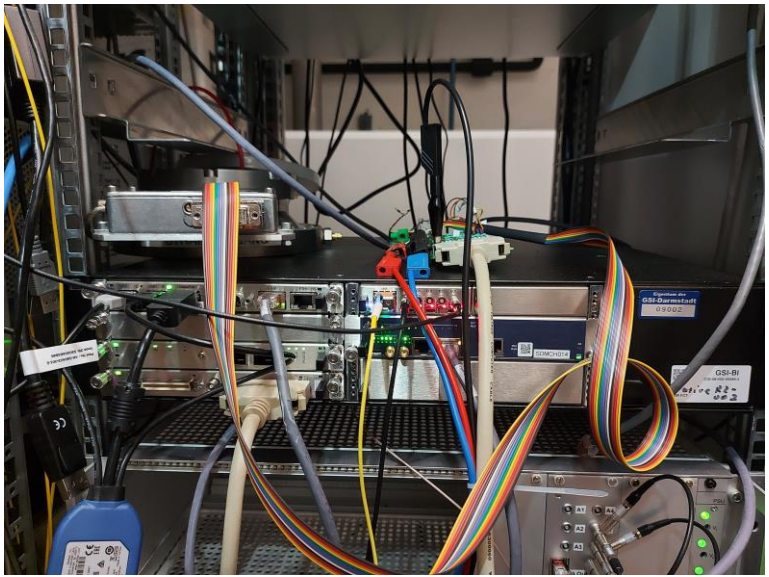
Software Status:

- DAQ chain from transformer/pre-amp in lab via driver up to GUI as draft expert version tested and functional
- Optimization of performance -> fulfills given requirements (10MHz, 5,5ms)
- Triggered readout (tested with simulated WR timing)
- User interface requirements from operation received



Hardware Status:

MAPS hardware at LSB 4 (X 5):

- 2U MTCA system with AM G64 CPU
- TAMC532 32 Channel ADC with RTM
- 2 x SIS8864 I/O Modules
- Fair Timing Receiver Node (FTRN)

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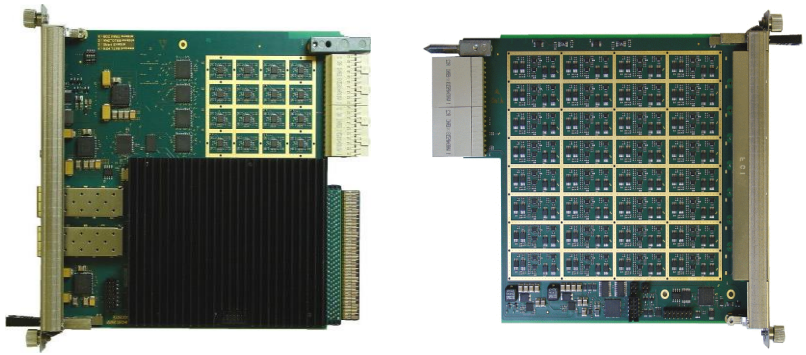
LSB4

LAN and WR installed

5 x TAMC-532 32 Channel ADC with input RTM



5 x MTCA.4 6-slot systems incl. CPU (Xeon), MCH und PS

10 x SIS8864 MTCA 64 Channel I/O Register

FAIR Timing Receiver Node (AMC)

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Next steps:

- Preparation of adaptor box
- First tests with beam (e.g. automatic range setting)
- Integration of LSA (e.g. charge state) and BTM system
- White Rabbit timing tests
- Realisation step-by-step, very many aspects and dependencies to old CS
- Set-up of U/f converter for SVÜ

Open issues:

- No solution for MAPS Oscilloscope yet, **if** 1GHz sampling is required
  - Plan A (easy): limited to 4 fixed signals, no switching and remote control of oscilloscope (LSB)
  - Plan B (expensive): switch matrix 64/4 to 1GHz DAQ or oscilloscope

- **Status now**: 10MHz is sufficient, higher resolution signals can be observed with phase probes and ion source oscilloscopes

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Efforts (estimated):

Task	Duration	Man power	Costs
Preparation of adaptor box:	3 - 6 months	0.25 FTE	10k€
Installation (step-by-step):	4 weeks	0.1 FTE	1k€ (cables, adaptors etc)
Programming basic FESA and GUI:	3 months	0.25 FTE	
Implementation additional features:	6 months	0.25 FTE	
SVÜ (preparation U/f converter boxes):	6 months	0.1 FTE	unclear

With adaptor box it is quite realistic to have MAPS 2022 operational in late 2022 early 2023.