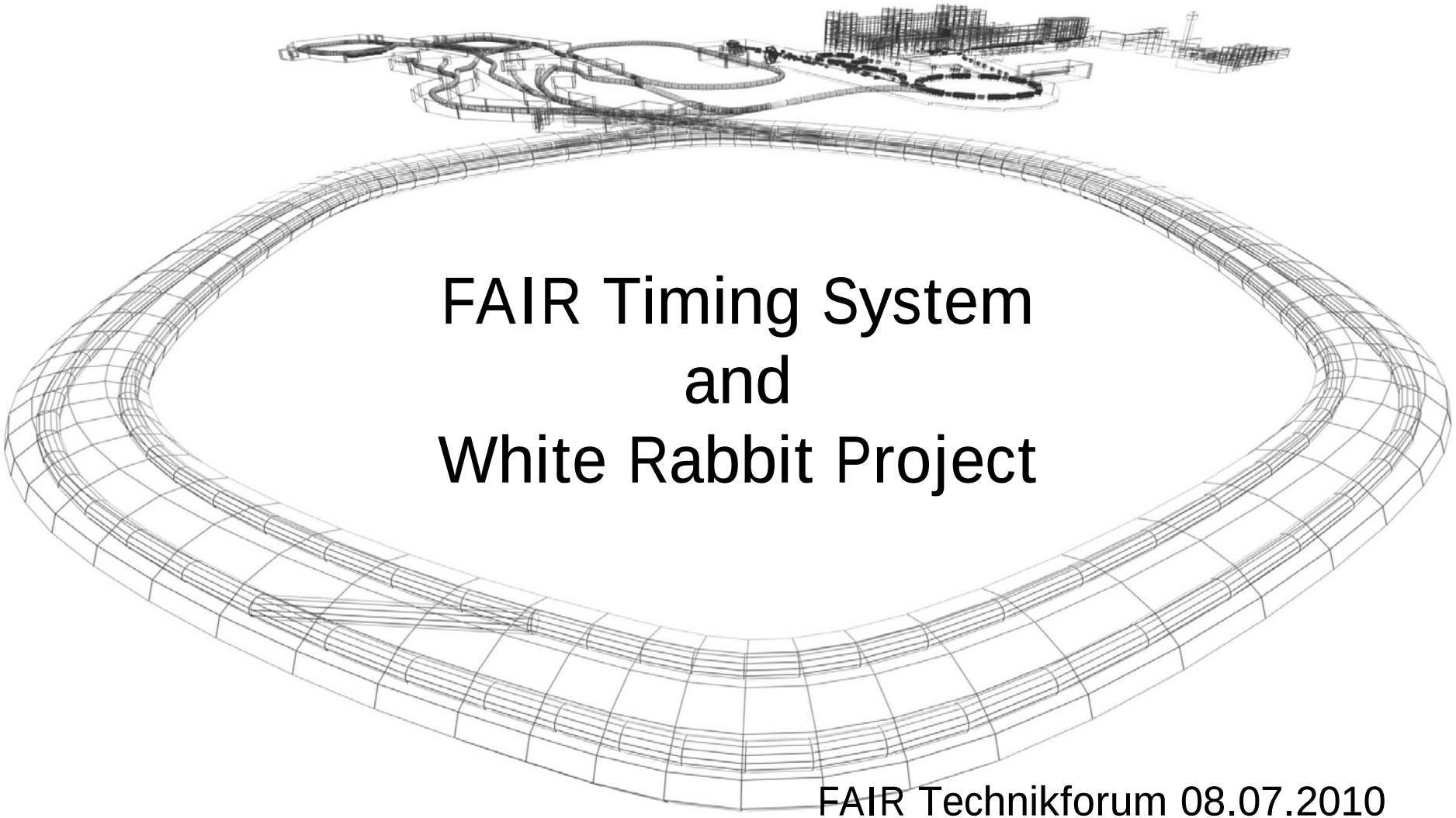


FAIR Timing System and White Rabbit Project

FAIR Technikforum 08.07.2010

Tibor Fleck / t.fleck@gsi.de

FAIR Timing System

Two distinct, yet tightly coupled systems:

General machine timing system

- BEL group
- distributes accelerator events
- distributes absolute time
- defines time standard for CS
- low ns accuracy / synchronization
- One global timing master

→ this talk

BuTiS (bunch phase timing system)

- HF group
- distributes high precision clocks for rf systems
- sub-ns accuracy / synchronization
- One global BuTiS center

→ future talk 28.10.

The WR Timing Project (started 2008 by CERN)

- Similar timing systems for different facilities
- Shared development / Open Hardware Repository
- Collaboration: CERN, GSI and others

  → CERN and GSI will use the same system / technology

What is "White Rabbit" ?

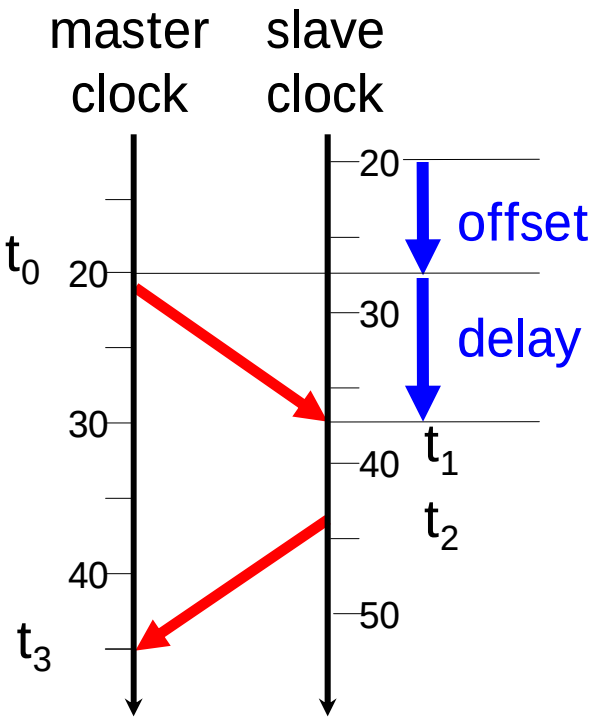
"White Rabbit is a fully deterministic **Ethernet-based** field bus for general purpose data transfer and synchronization. […] The key technologies used are **Synchronous Ethernet** and **PTP** (IEEE1588)."

- WR protocol – special layer 2 "WR switches" / "WR nodes"
- Precise time and frequency transfer
- Deterministic frame transmission / fixed switching latency
- High robustness: event loss <~10^{-15}

FAIR Timing System

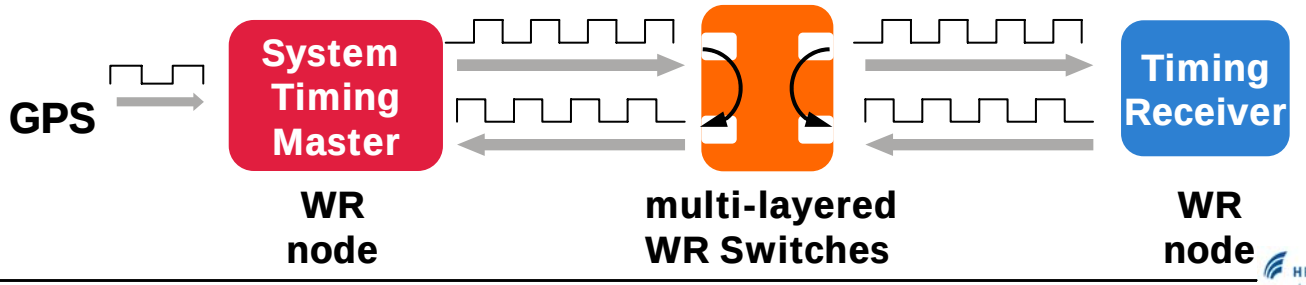
Precision Time Protocol (→ deliver time of day)

- Use WR handshakes and exact timestamping
- Synchronize local times with master time
- Measure and compensate link delays



Synchronous Ethernet (→ deliver frequency)

- Nodes use same physical clock
- Clock encoded in Ethernet carrier
- Clock recovered by PHY PLL



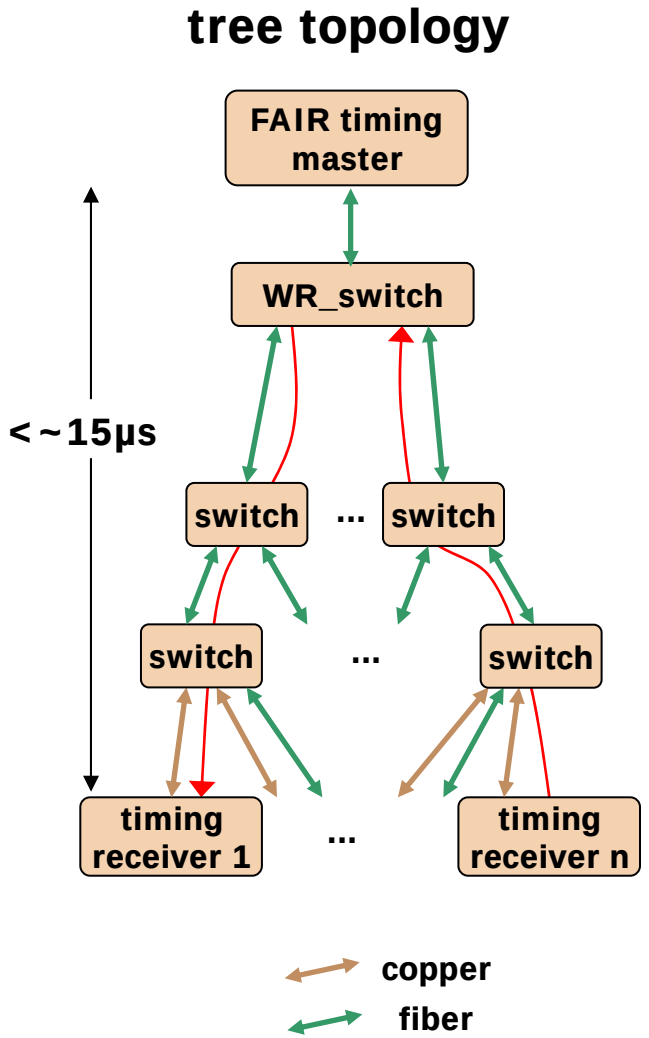
FAIR Timing System

Features

- Timing events broadcasted facility-wide
  - → Events bundled for transmission
  - → Encoded / "repeated" for robustness
  - → Distribution every 100µs
  - → Distribute event execution times

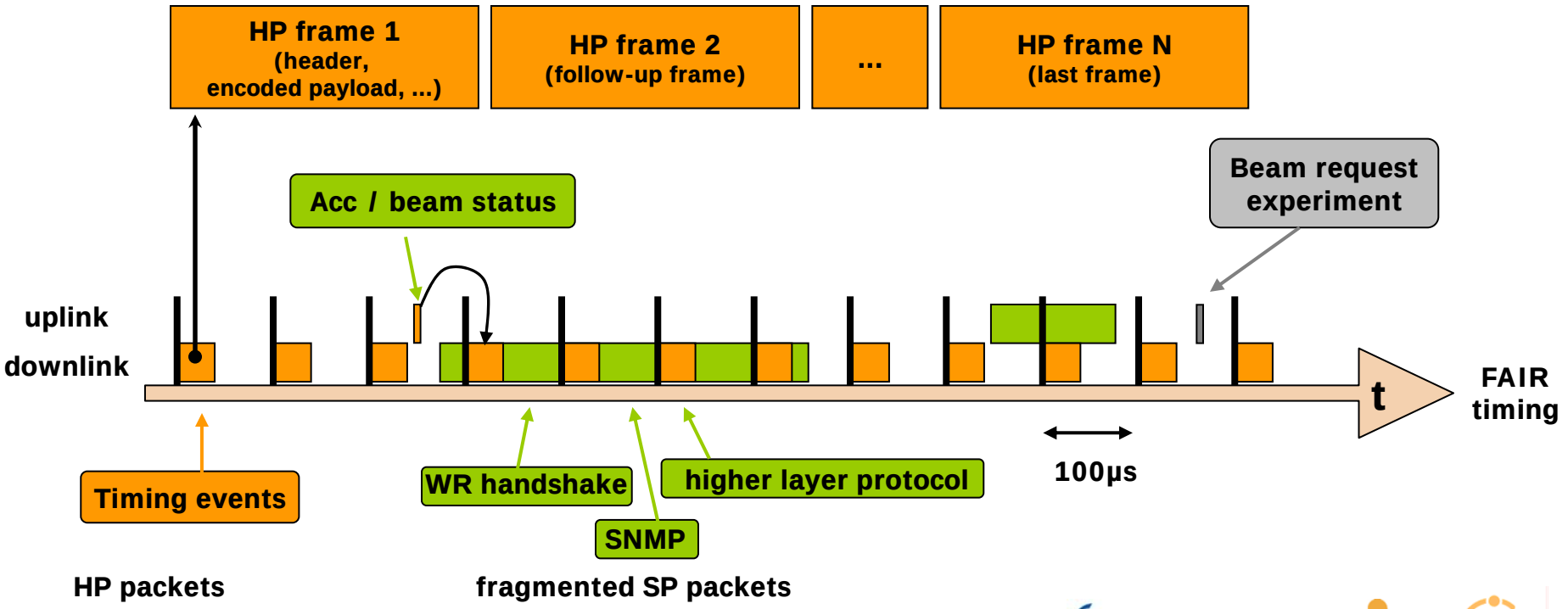
event stream header	event 1	...	event N	Acc / beam status info

- Deterministic delay, high reliability
  - → high priority "HP" packets
- <~200 WR switches
- ~ 2000 timing receivers

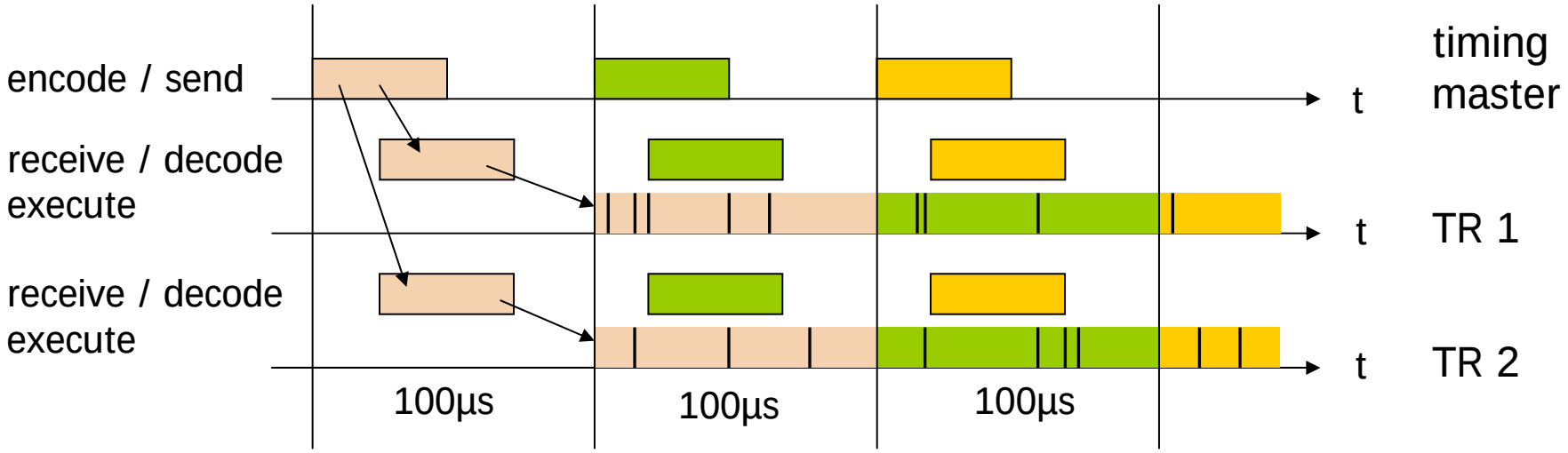


Event distribution

- Not purely event based !!
- Forward error correction algorithms

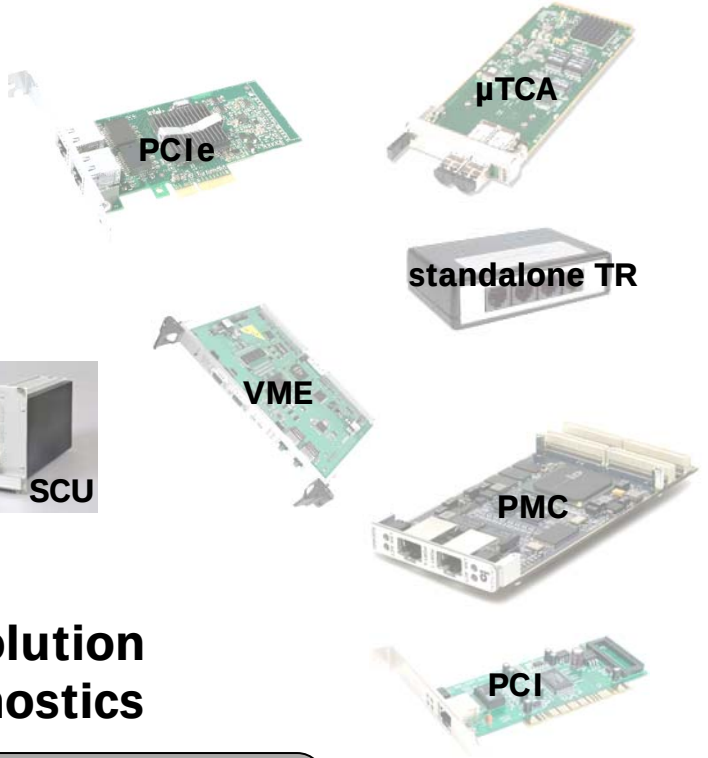


Event distribution

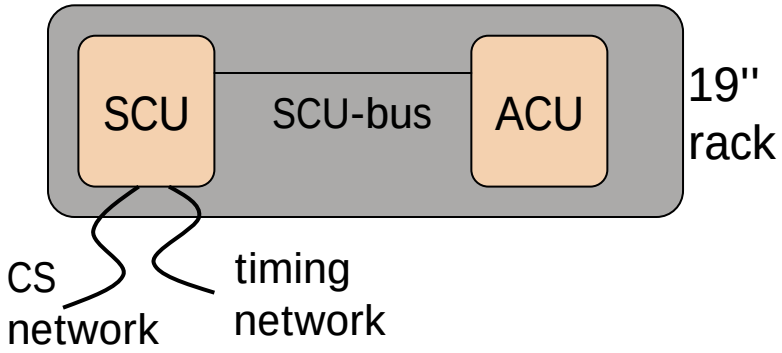


WR Timing Receiver (TR) Boards

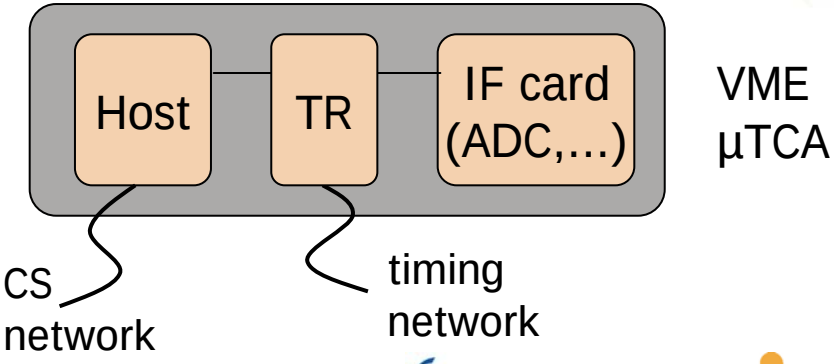
- Event decoding, postprocessing and filtering
- Absolute notion of time
- Optional Mezzanines on FMC carriers !
- Form factors:
  - → SCU (standard FAIR controller)
  - → VME, PCIe, µTCA, standalone TR
- Full FESA device integration / Linux driver



standard solution power supplies



standard solution beam diagnostics



Main enhancements vs. current timing system

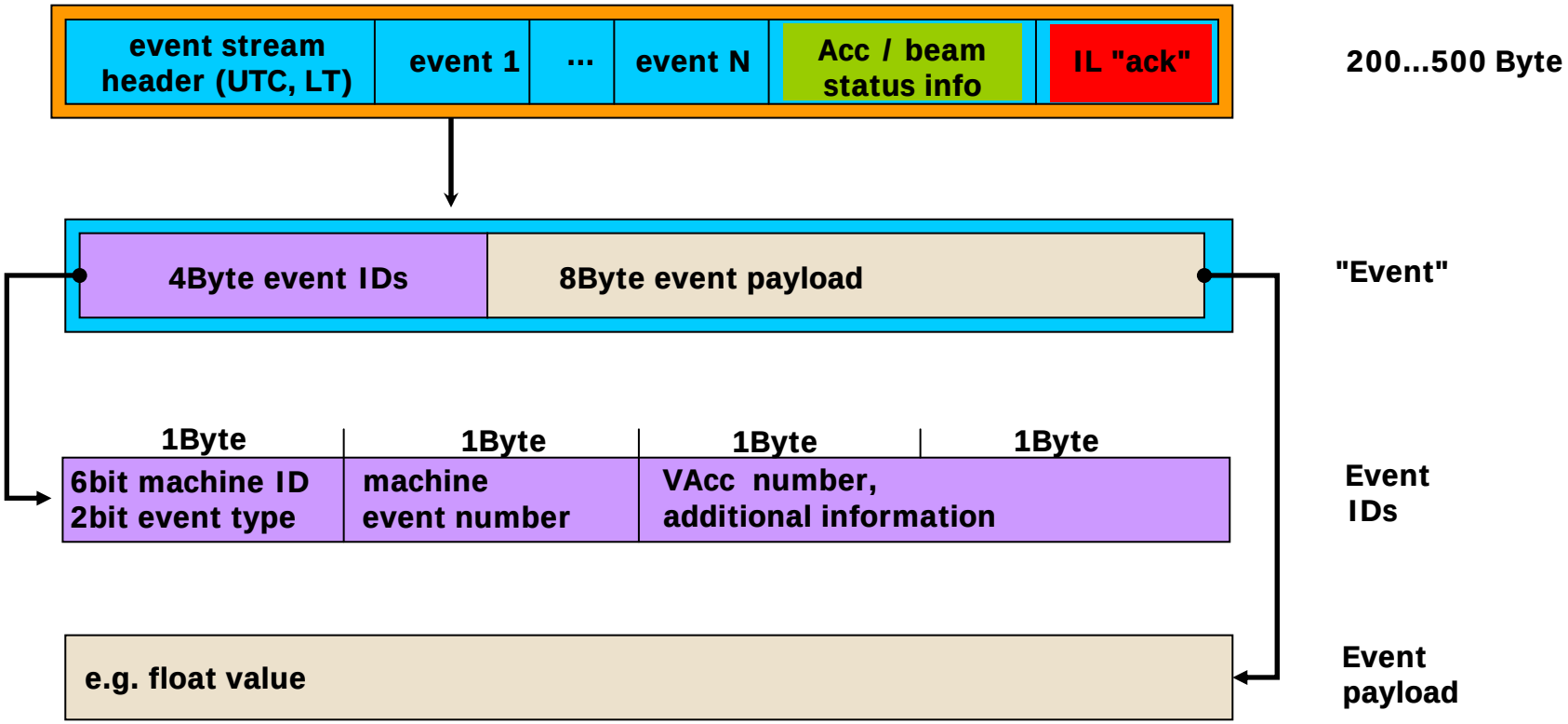
- Absolute (UTC related) notion of time in all TRs
- Parallel event execution / no minimal event separation
- Bidirectional communication possible (node → master)
- Huge bandwidth / facility-wide event distribution
- Large event content (4 Byte header info / 8 Byte payload)
- Transmission of frequencies possible (→ BuTiS 100kHz clock)
- Potential to be used for further deterministic and reliable communication
  → online beam information, interlock transmission … 2 b explored

Thanks for your attention...

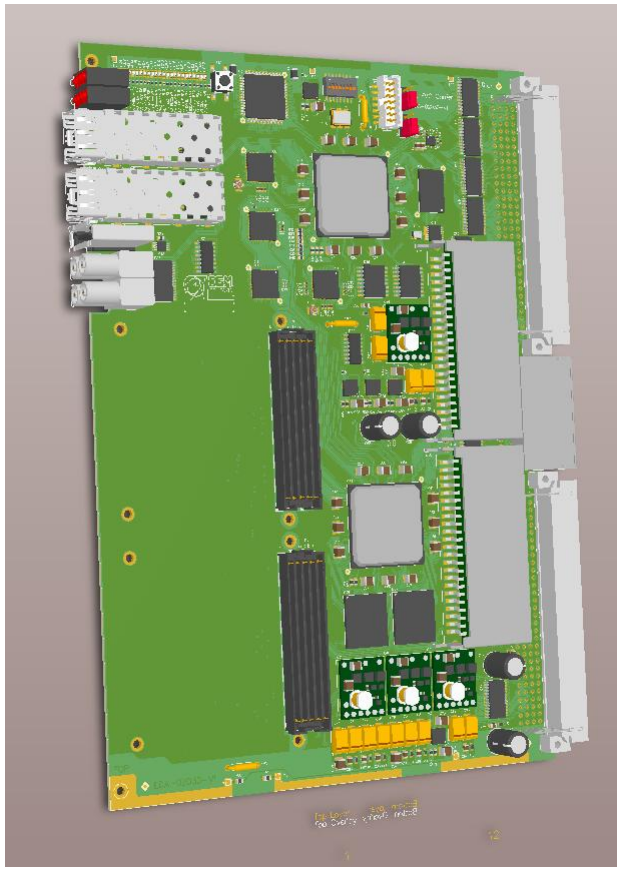
... let's have some good discussion now

→ it's still possible to have some influence on the concepts

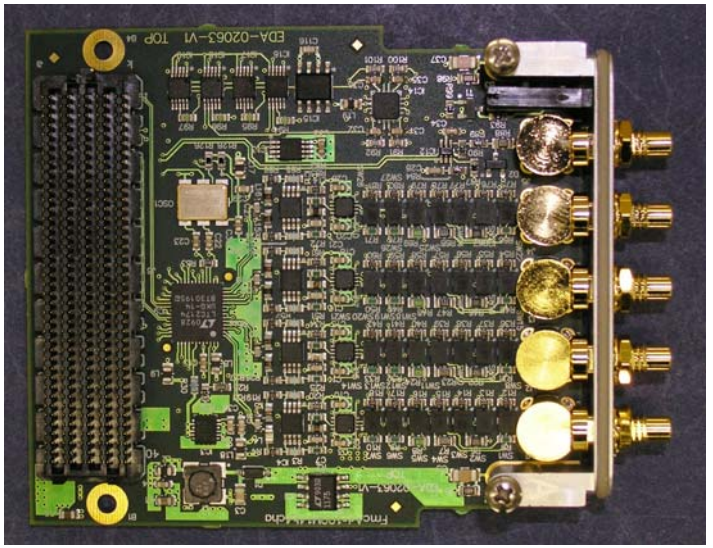
Event packet content



VME timing receiver



4 channel 100MSPS 14 bit ADC mezzanine card



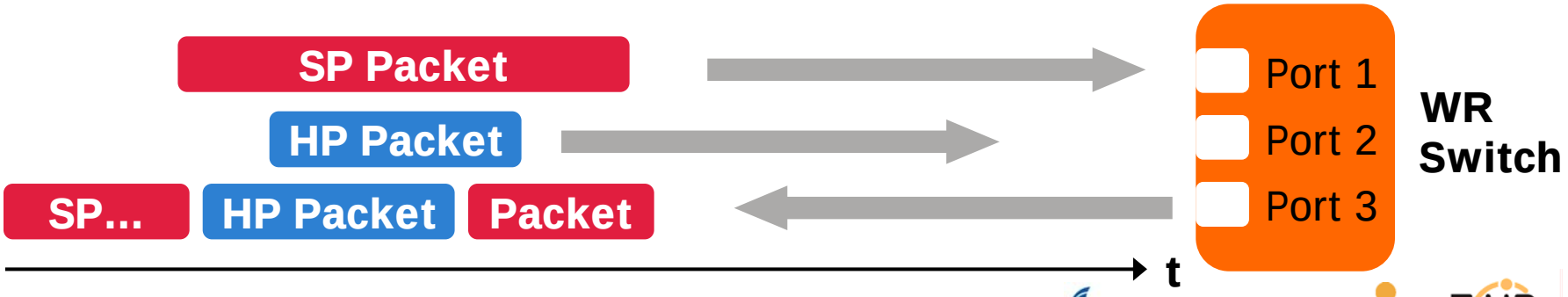
White Rabbit Protocol

- Ethernet traffic split into:

  High Priority (HP) packets
  Standard Priority (SP) packets

- HP packets use special value Ethertype field in frame

- HP packets preempt other packets „on-the-fly”



FAIR Timing Master

- Central powerful hardware
- Fully FESA compliant device
- Real time parallel event scheduling in FPGA
- Event stream generation / encoding

WR Timing Switches

- PTP handling
- Layer 2 port management
- Precise timestamping
- High precision clock / phase measurement

FAIR Timing System
BuTiS Integration

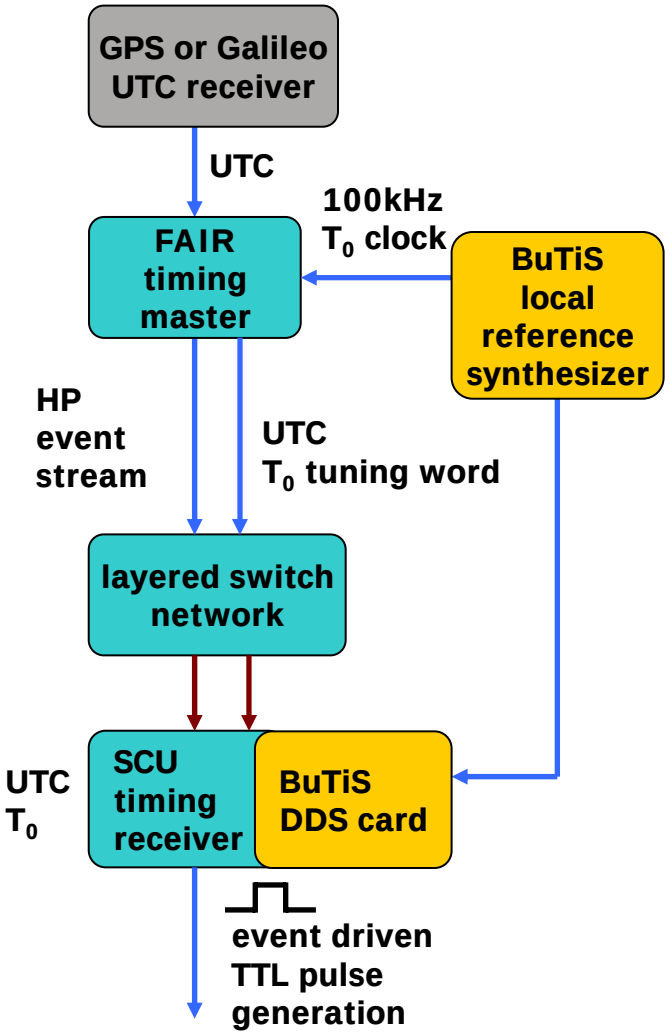
BuTiS Architecture:

- High precision 10/200MHz rf clocks
- 100kHz clock

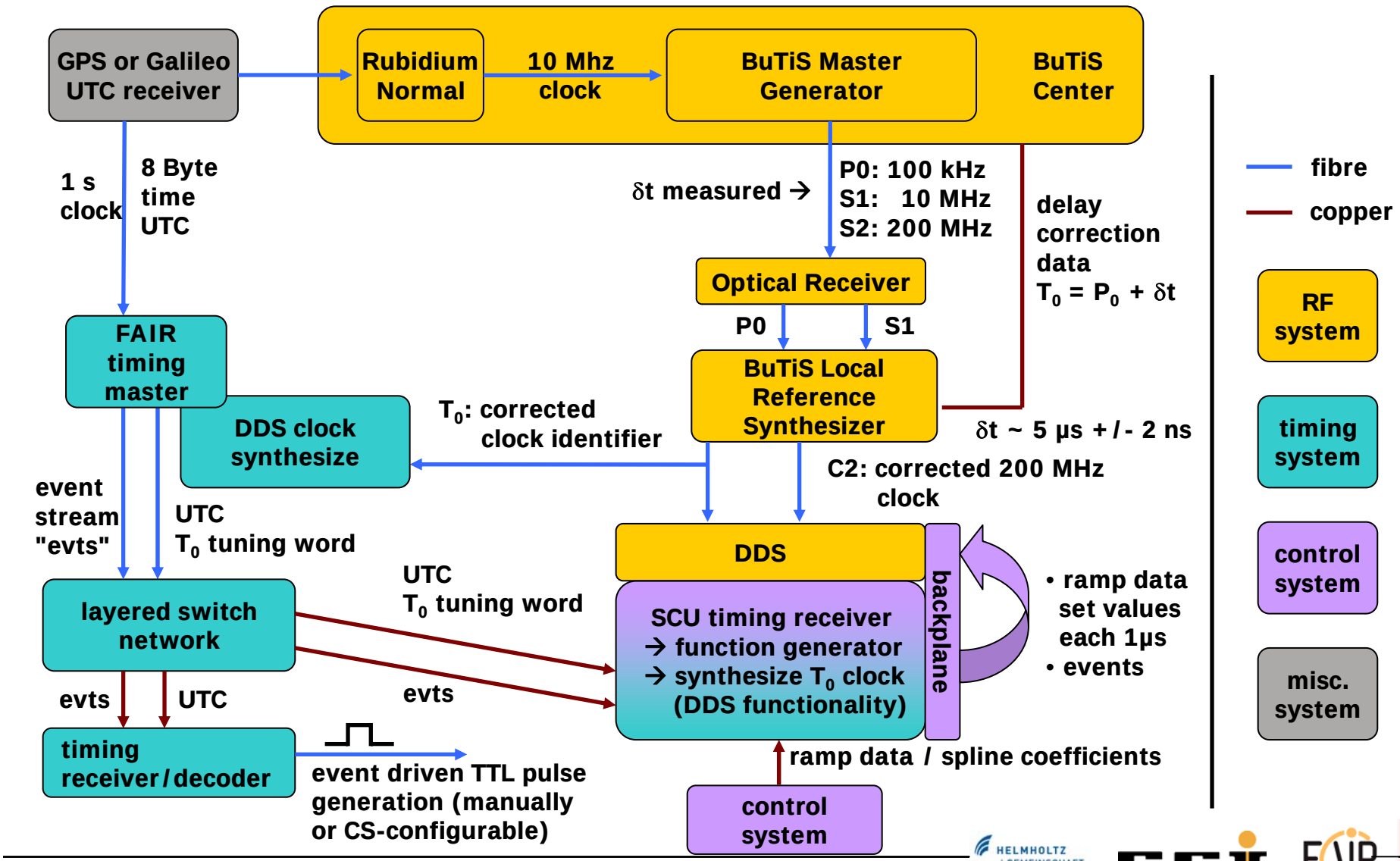
Problem: different time domains

Solution: Distributed DDS

- Timing Master samples BuTiS clock
- Timing network fully transparent to BuTiS clock
- Distribution of „tuning words“
- Timing receivers resynthesize 100kHz BuTiS clock
- Accuracy < 1ns



Correlation between the rf BuTiS system and the timing system at FAIR



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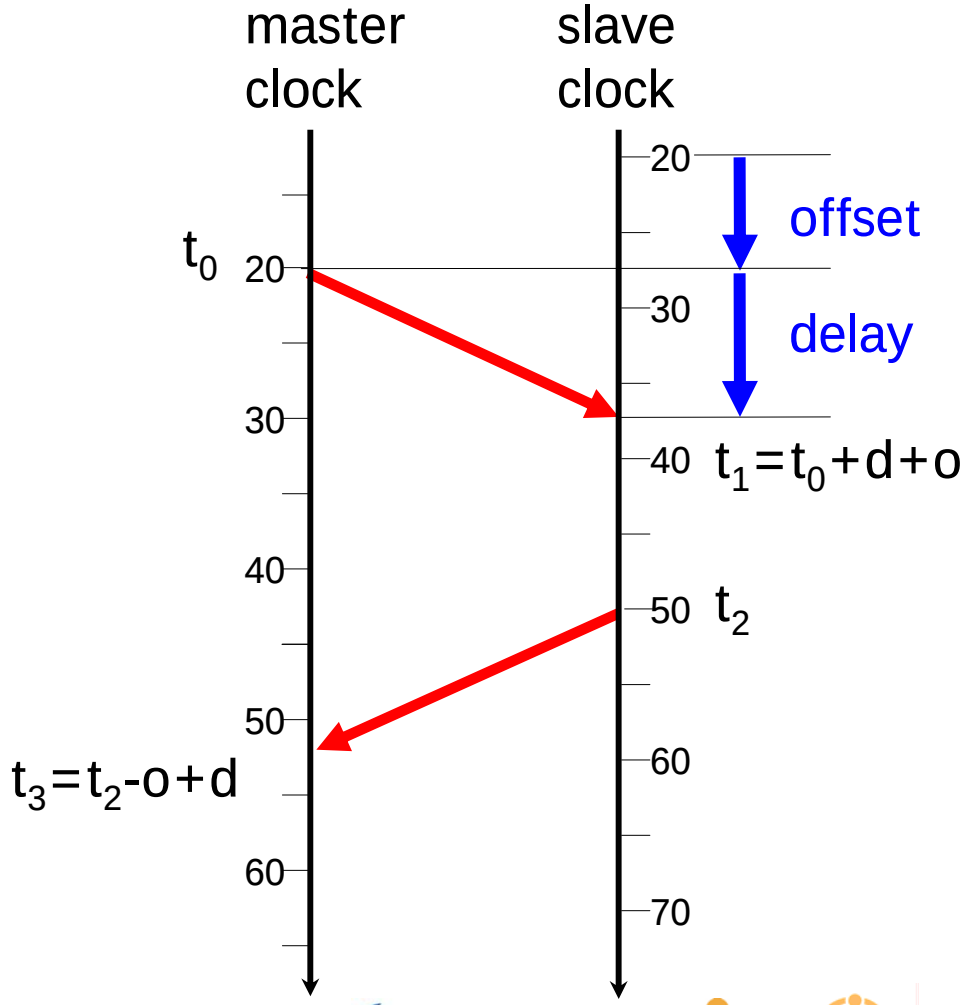
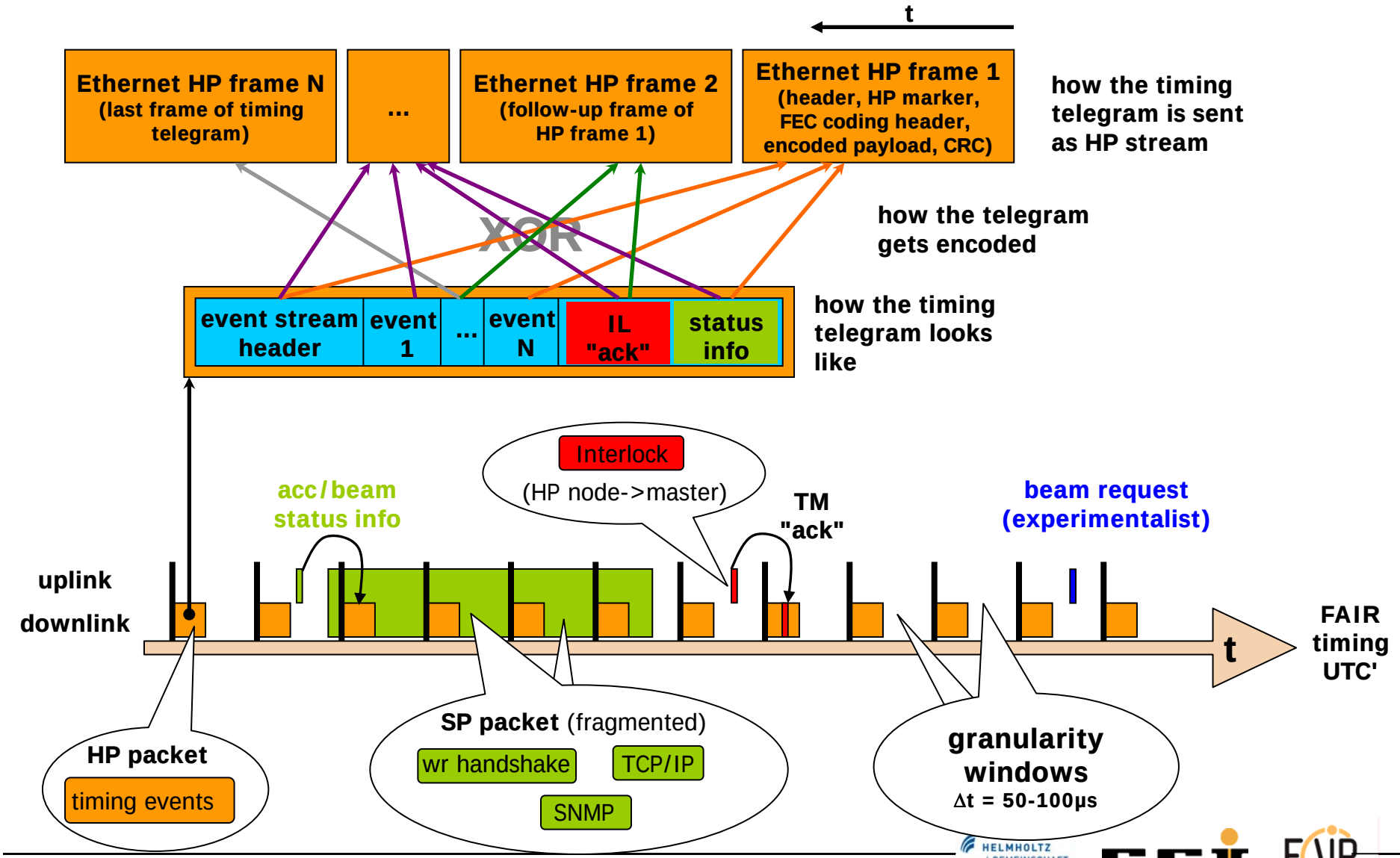


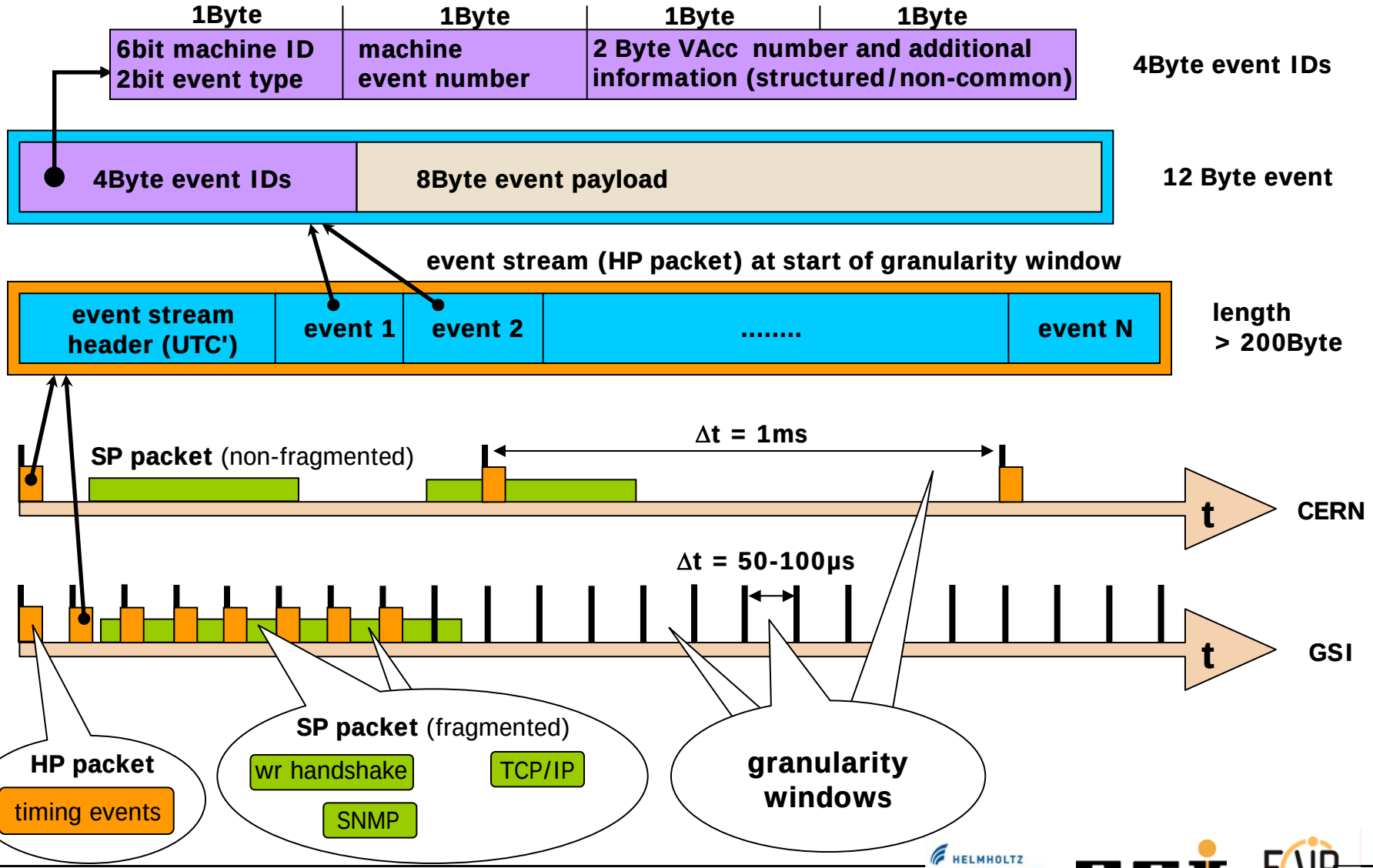
$$d = \frac{(t_1-t_0)+(t_3-t_2)}{2}$$

$$o = \frac{(t_1-t_0)-(t_3-t_2)}{2}$$

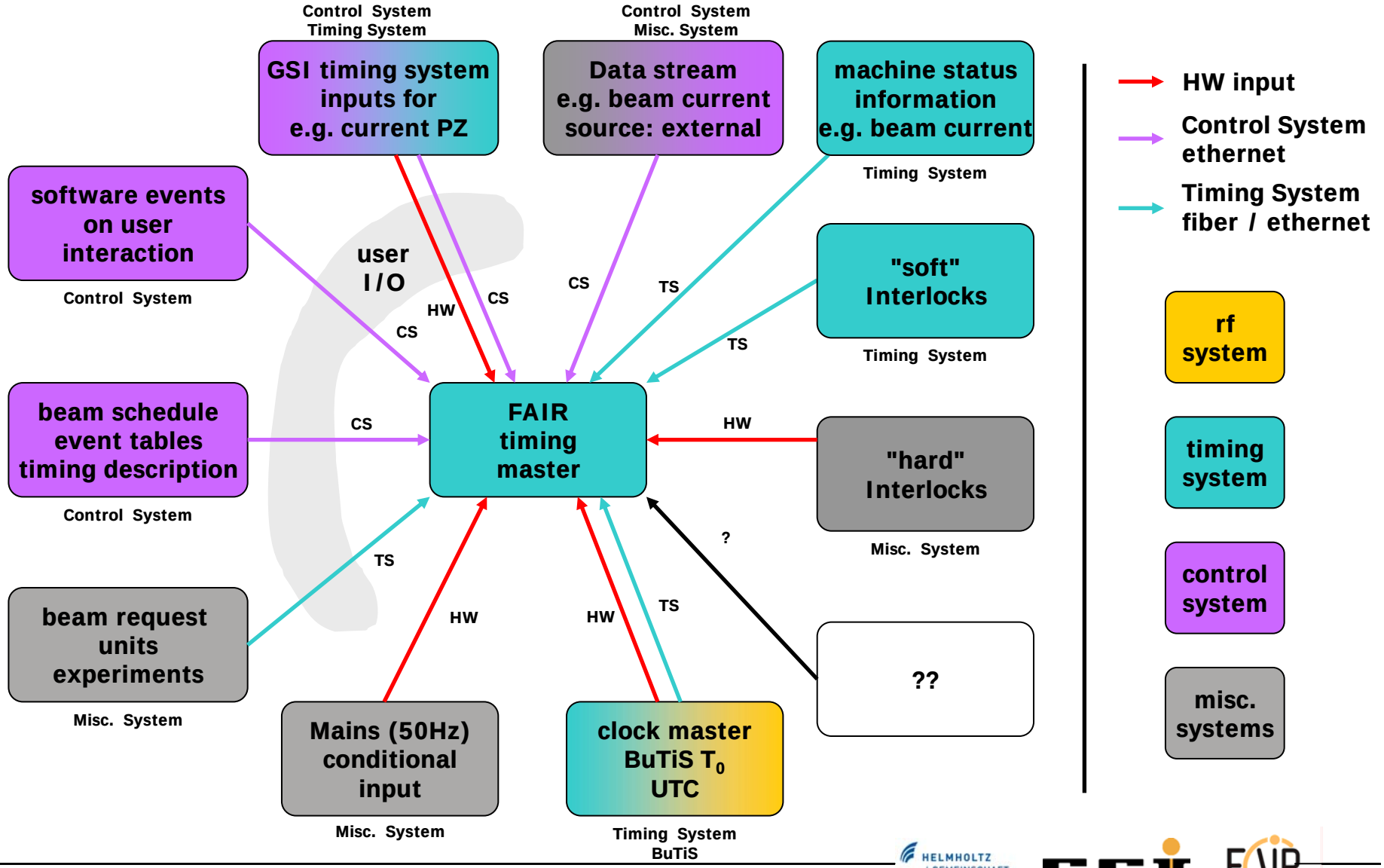
timing event messages
granularity windows concept



timing event messages / content
granularity windows



timing master inputs



timing master outputs