Component:	IFC(3) and VDIO	**Project**	SIS18 spill counter retrofit
Document:	long cables / signal buffer with pre-emphasis	**Date**	05. 02. 2019
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1 Situation

The input currents of the ubiquitous IFC(3)s are delivered by beam collimators, SEETRAMs or ICs, and converted into a linearly proportional pulse rate by the IFCs. These pulses are then transmitted from the instruments located along the HEST beam lines by internal RS485 transmitter ICs (MAX485 or MAX3291) to the DAQ station in BG2.009/ELR, over long twisted pair cables. If the cable length significantly exceeds ~100m, pulse amplitude and edge speeds are reduced by the cable's ohmic and dielectric losses, and in turn pulse discrimination by the RS485 receivers in the V-DIO's input stages is no more reliable. In order to improve the signal fidelity, a corrective measure had to be developped, in form of a little adapter box placed between the VDIO's DSub15 input socket and the DSub cable plug. As 12V DC power is available on 2 lines of the cable, an active electronic circuit like a buffer or discriminator circuit was obvious.

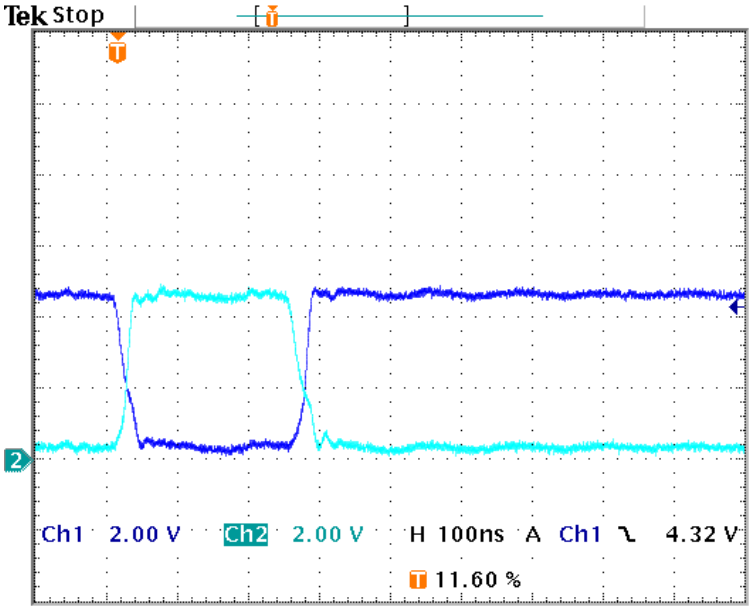

Fig. 1 pulse shapes with 120 Ω terminator dirctly at IFC3 differential output

Fig. 1 shows the differential pulse signals, taken at a 120Ω termination resistor directly placed at the outputs of an IFC3. All levels are inside the TTL specification, with rise and fall times in the 10ns range. The voltage overlap is sufficiently above the differential threshold (~150mV) of the SN65HVD75 RS 485 receiver [3] in the VDIO's input circuit, so the receiver will discriminate the pulses by 100%.

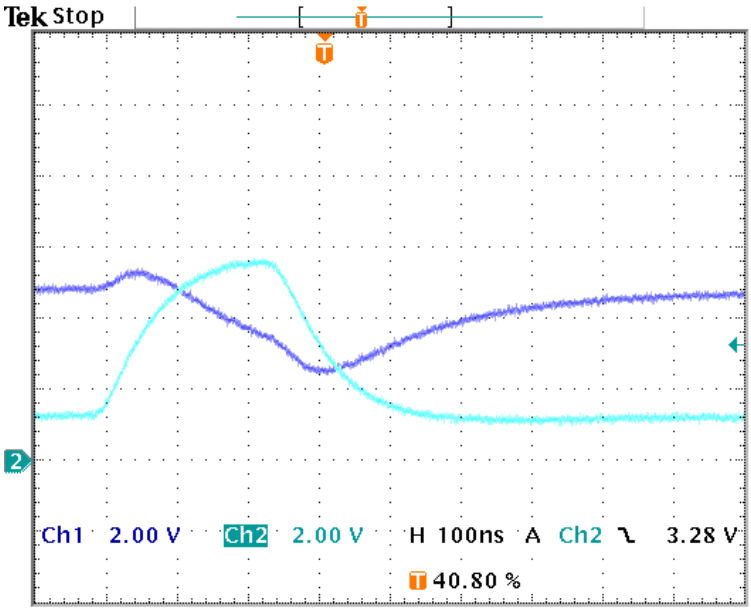

Fig. 2 pulse shapes with 120 Ω terminator after ~100m twisted pair cable (lab experiment)

The situation gets really worse if a cable of ≥100m length is placed between IFC and VDIO, see Fig. 2. Especially the inverted output of the RS485 transmitter is significantly distorted, while both pulse edges are considerably degraded. With a further increased cable length, the amplitude of the noninverted output will be again reduced due to the increased dielectric losses i. e. low pass filter effect, and pulse discrimination by the receiver gets unreliable.

2 Solution

Ref. [1] describes a method to improve the pulse fidelity and amplitude of the differential RS485 signals by inserting a true differential operational amplifier into the signal path. By slightly increasing the DC gain and introducing an equalization or pre-emphasis in the appropriate frequency band, the cable losses can be compensated and the pulse shapes be improved, so no pulses are lost anymore.

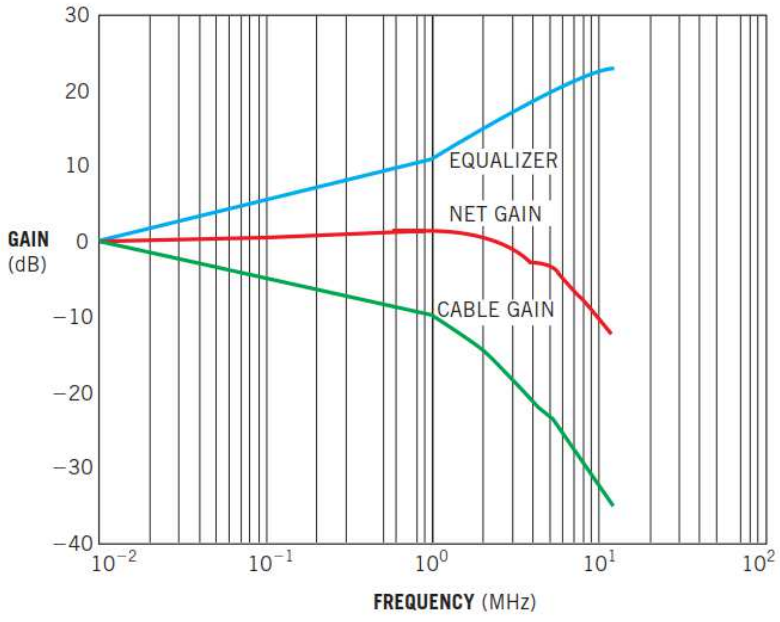

Fig. 3 compensating cable losses by a frequency-matched equalizer gain (from [1])

3 Realization

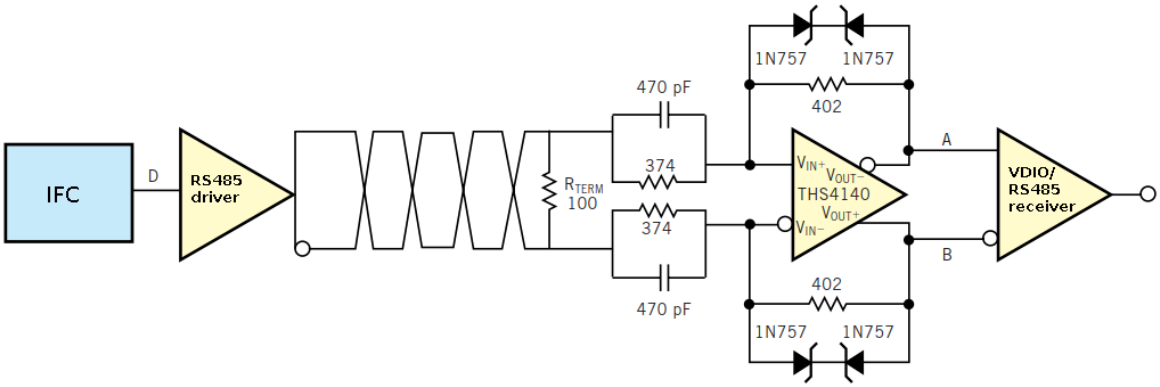

Fig. 4 basic cable buffer with pre-emphasis (from [1], R and C values exemplary)

The basic circuit (Fig. 4) was adapted from [1]. The THS4140 will be powered from the single 12V interface supply, which fortunately is present on 2 lines of the cable. In order to keep the common mode output voltage below the VDIO's input receiver safety level of ~7V [3], an appropriate resistor was connected from the amplifier's V_{ocm} input (not shown in Fig. 4, see Fig. 5) to $-V_{cc}$. Limiting zeners keep both ouitputs below the permitted differential safety level.

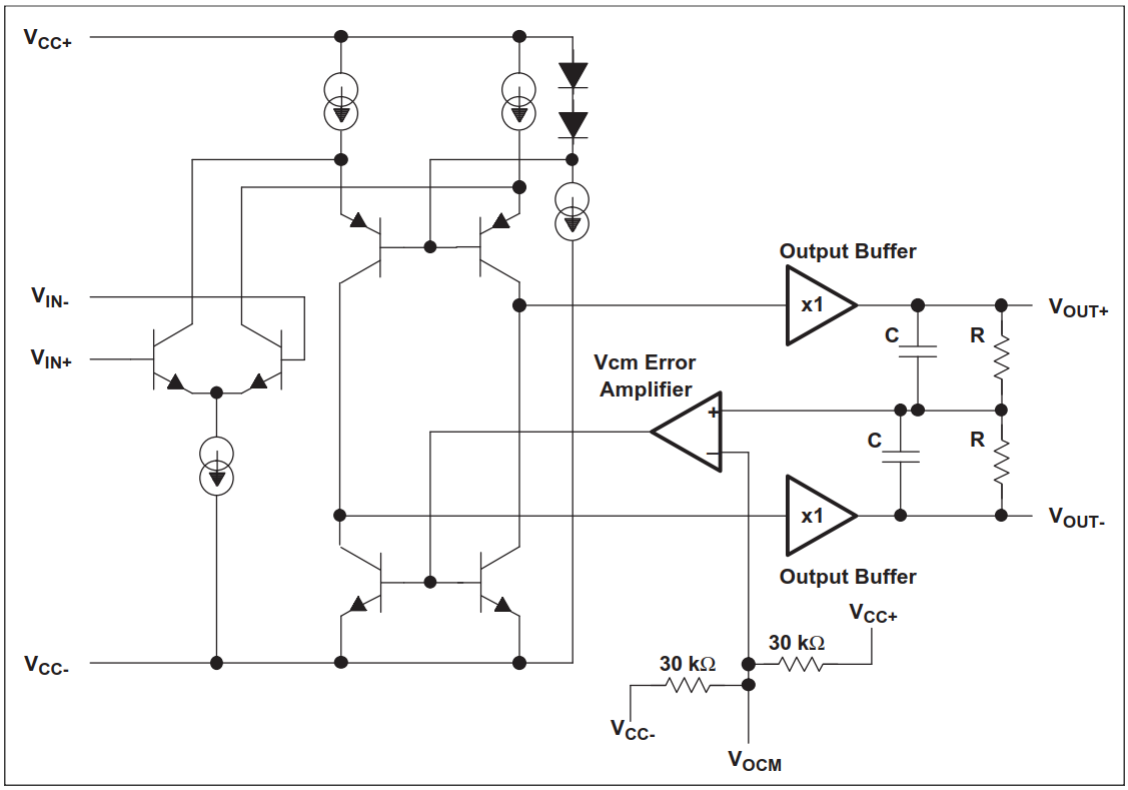

Fig. 5 simplified diagram of THS4140 (from [2])

Fig. 6 depicts the equalized pulses, captured directly at the IFC's output, terminated with 120Ω.

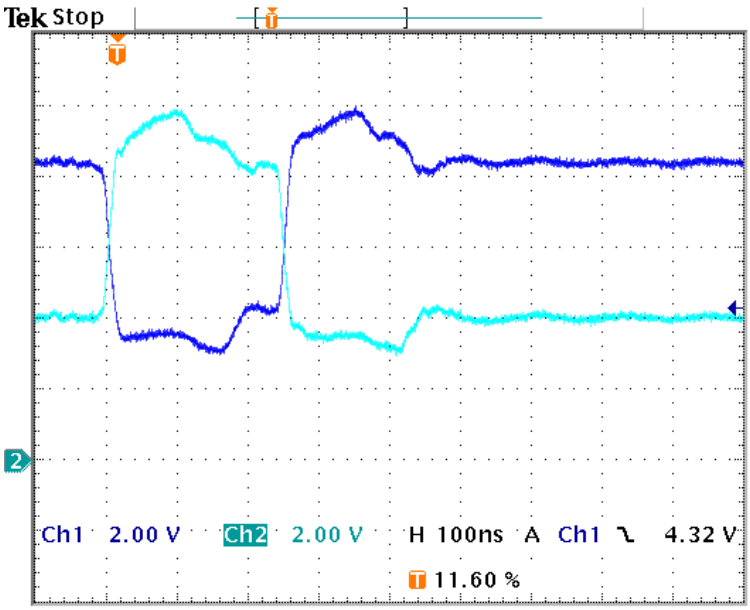

Fig. 6 pulse shapes @ 120Ω termination connected at the IFC's output pins through the pre-emphasis buffer

The circuit was realized on a small double-layer PCB, which was soldered between two 15p DSub connectors, male and female, respectively. The overall distance of the connectors / PCB was chosen so that the unit fits into a 15p-DSub clamshell box.
Because the adapters later will be mounted inside 19" racks and staying there unattended for years, a safe and reliable operation on a long term scale must be provided. As the amplifier chip is a broad band device, it's quiescent current and hence the power dissipation are quite high and might shorten the component's MTBF. An operation temperature as low as possible should be achieved.
While the PCB was still on the lab bench, not mounted in the closed adapter shell, the chip's surface temperature was measured under typical working conditions (~50 kHz pulse rate, std. RS485 termination). Fig. 7 shows that >70°C are present in the chip's center.

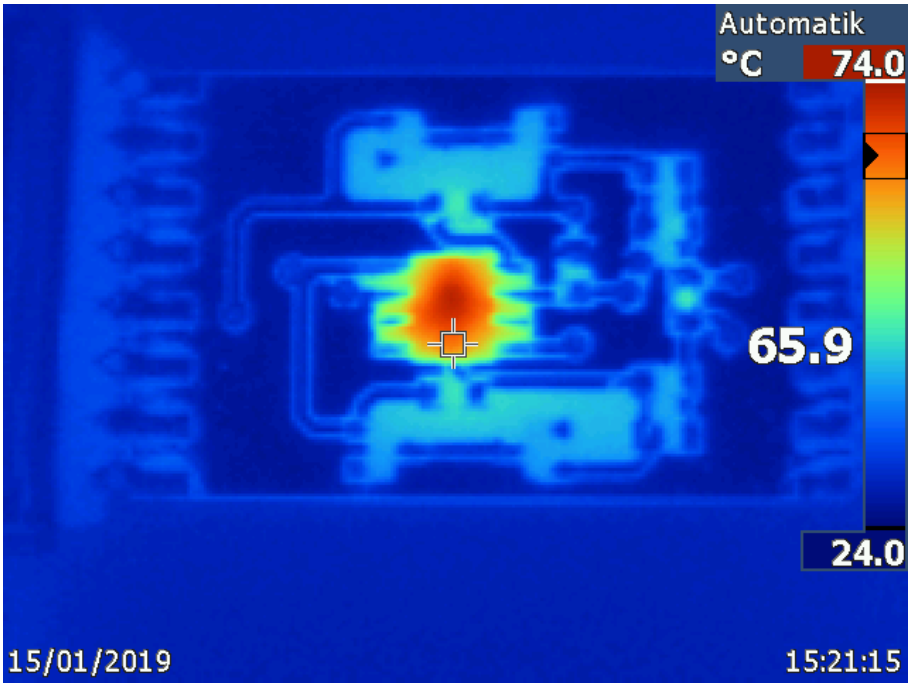

Fig. 7 surface temp. of THS4140, PCB in free air

4 Results

To reduce the temperature, a small blackened heat sink was attached on top of the chip, using thermo-conductive glue. Of course this required an orifice for the cooling fins in the adapter's top shell.

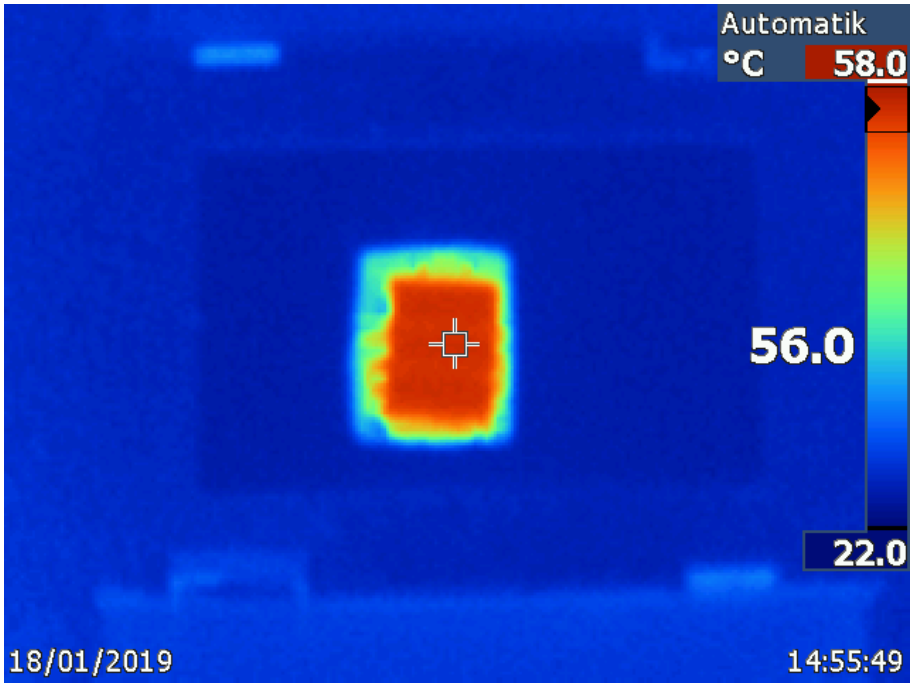

Fig. 8 temp. of heat sink, with PCB inside closed adapter shell

Finally, the opening around the heat sink was slightly enlarged, and holes of 4mm diameter were drilled into both side faces of the upper adapter shell, enabling slight air convection. The (acceptable) result is shown in Fig. 8.

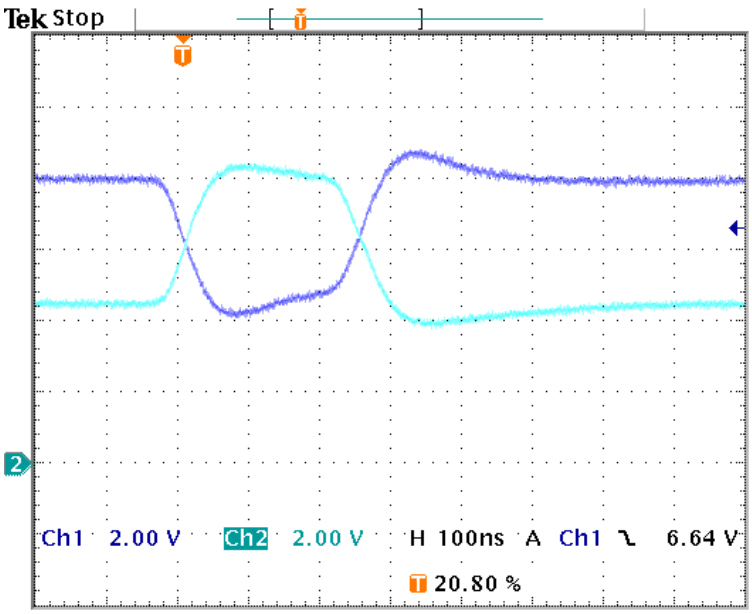

Fig. 9 pulse shapes after ~100m twisted pair cable, with 120Ω termination and the pre-emphasis buffer

Fig. 9 depicts the strongly improved pulse fidelity, while the common mode voltage is still too high and may damage the VDIO's input circuitry.

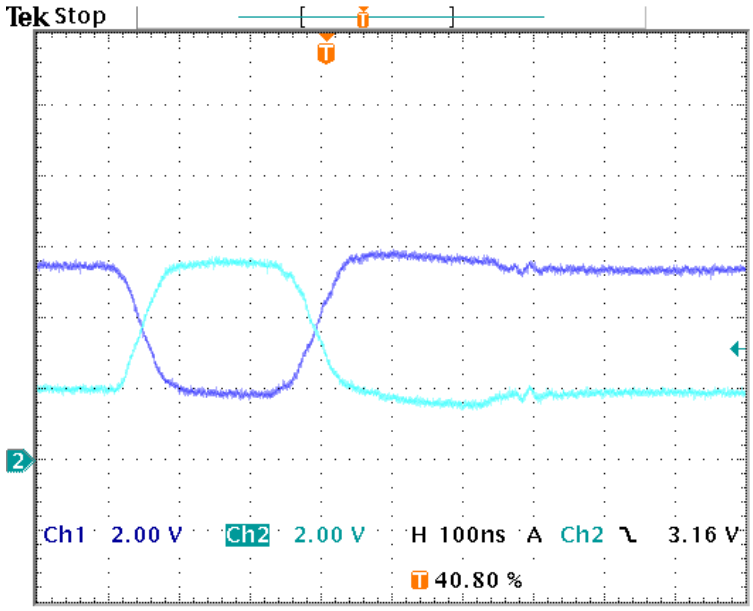

Fig. 10 same as Fig. 8, common mode voltage reduced

Fig. 10 shows a pair of well restored pulses for the VDIO's input, with rise/fall times in the 20-30ns region; the output common mode voltage is safely reduced by adding a resistor at the V_{ocm} input of TSH4140.

Fig. 11 depicts the initial situation when used in the real accelerator world. The yellow and blue traces show the differential RS485 pulses, the red trace the sum of these. Due to insufficient signal overlapping, many counter pulses are missing.

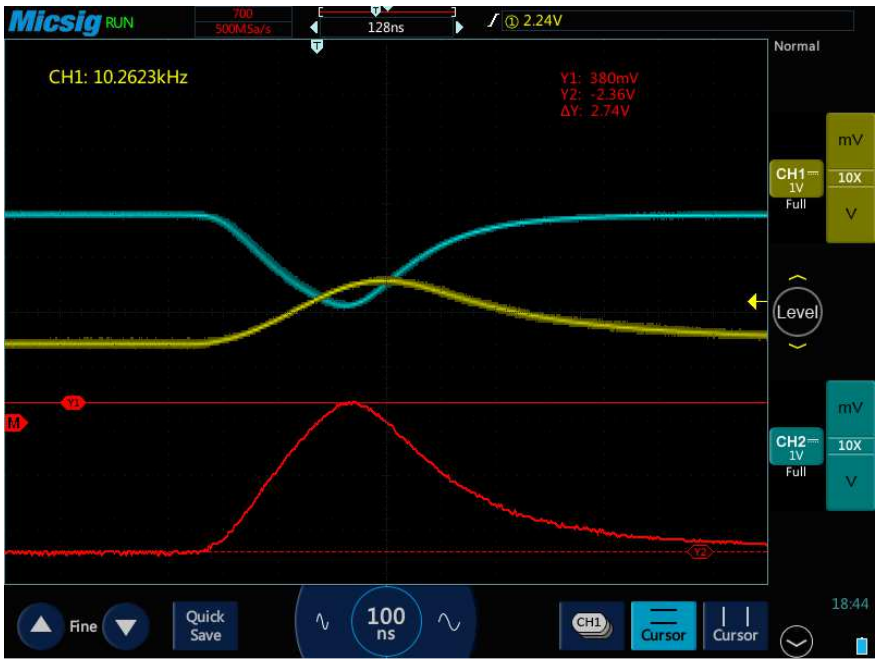

Fig. 11 pulse shapes, terminated after ~200m twisted pair cable (HADES beam line)

The Fig. 12 shows the buffer's impressive effect. It was inserted into the HADDI3I DAQ line, just in front of the dedicated VDIO. The actual cable length was ~200 m. Surprisingly, and contrary to the receiver's datasheet, a minimum pulse overlapping of ~700mV had to be exceeded.

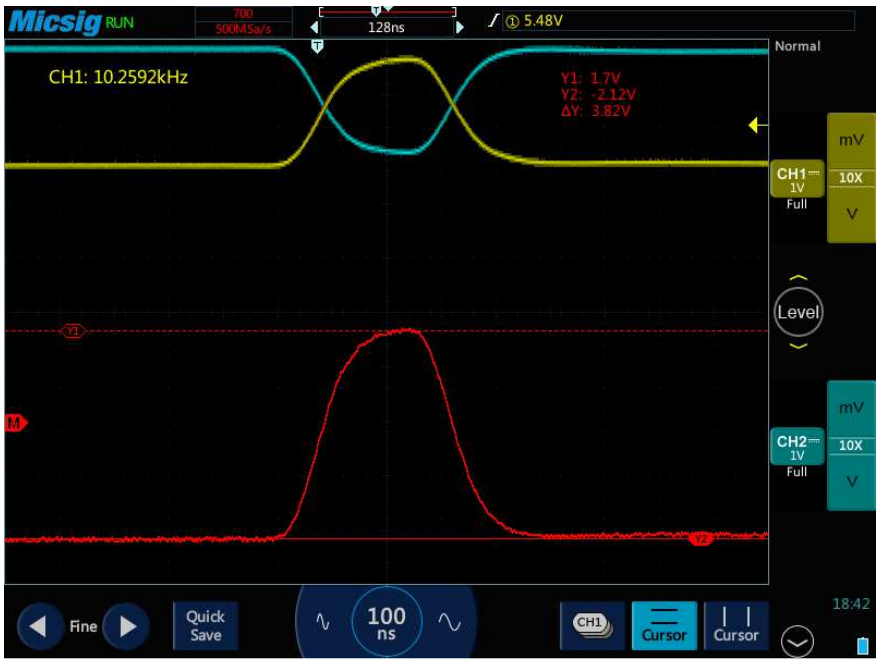

Fig. 12 pulse shapes after ~200m twisted pair cable, pre-emphasis buffer added (HADES beamline)

Table 1 lists the actual values of the electronic components:

C1, C2	HF boost	470 pF
R1	termination	100 Ω
R2, R3	Input	360 Ω
R4, R5	feedback	390 Ω
R6	ocm correction	27 kΩ
D1 – D4	output limiter	BZX84C9V1
IC1	diff. op amp	THS4140

Table 1 component values

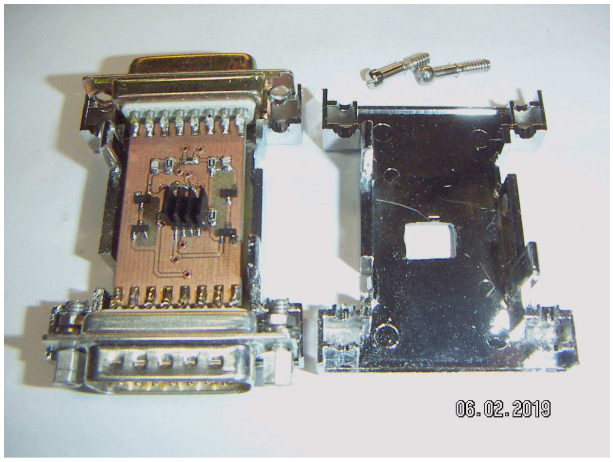

Fig. 13 adapter prototype, upper shell opened

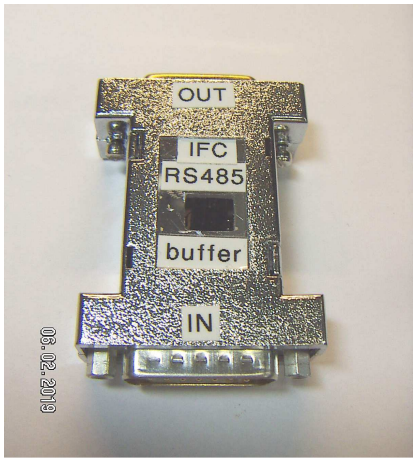

Fig. 14 adapter, top view

The adapter is now ready for production of a small batch of 20 pieces.
It can also be used for FAIR spill counter systems.

5 References

[1] https://www.edn.com/design/industrial-control/4013759/Increasing-RS-485-Networking-via-Receiver-Equalization?utm_source=eetimes&utm_medium=networksearch
[2] http://www.ti.com/product/THS4140
[3] http://www.ti.com/product/SN65HVD75