SIS3820
VME Output Register
with IRQ functionality

User Manual

SIS GmbH
Harksheider Str. 102A
22399 Hamburg
Germany

Phone: ++49 (0) 40 60 87 305 0
Fax: ++49 (0) 40 60 87 305 20

email: info@struck.de
http://www.struck.de

Version: sis3820-M-F301-1-v100-32out.doc as of 26.11.12

Revision Table:

Revision	Date	Modification
0.01	20.11.12	derived from SIS3820 F001
1.00	26.11.12	First official release

1 Table of contents

1 Table of contents 3
2 Introduction 5
3 Technical Properties/Features 6
4 Functionality 7
4.1 Block Diagram 7
5 Getting started 8
5.1 Installation 8
6 VME Addressing 9
6.1 Address map 10
7 Register description 11
7.1 Control/Status Register(0x, write/read) 12
7.1.1 Enable/disable counter bits 13
7.1.2 Invert/don't invert control input bits 13
7.1.3 Invert/don't invert control output bits 13
7.1.4 Flipflop enable 14
7.2 Module Id. and Firmware Revision Register (0x4, read) 15
7.2.1 Major and minor revision numbers 15
7.3 Interrupt configuration register (0x8) 16
7.3.1 IRQ mode 16
7.4 Interrupt Control/Status register (0xC) 17
7.5 Output data registers (0x10 and 0x14/0x18) 19
7.5.1 Direct output data register (0x10) 19
7.5.2 J/K output data register group 1 (0x14) 20
7.5.3 J/K output data register group 2 (0x18) 21
7.6 Counter registers 0x30,0x34, 0x38, 0x3C 22
7.7 Clear counter register 0x40 22
8 Front panel elements 23
8.1 Front Panel Layout 23
8.2 Front Panel LEDs 24
8.3 Flat cable Input/Output Pin Assignments 25
8.3.1 ECL 25
8.3.2 TTL 26
9 Board Layout 27
10 Jumper settings/pinouts 28
10.1 J1 28
10.2 J90 28
10.3 JP570 JTAG source 29
10.4 CON500 JTAG 29
11 Input Configuration 30
11.1 ECL 30
11.2 LVDS 31
11.3 NIM 32
11.4 TTL 33
11.4.1 TTL/LEMO 33
11.4.2 TTL/Flat Cable 33
12 Appendix 34
12.1 P2 row A/C pin assignments 34
12.2 Row d and z Pin Assignments 35
12.3 Connector Types 36
12.4 Power consumption 36
12.5 Operating conditions 36
12.5.1 Cooling 36
12.5.2 Hot swap/live insertion 36
12.6 LED (selftest) 36

13 Index 37

2 Introduction

The SIS3820 is a multi purpose counter/digital I/O board. This document describes the SIS3820 output register hardware/firmware combination. It can be seen as a combination of the SIS3600 output register implementation and 4 channels of scaler on the control/interrupt channels.

3 Technical Properties/Features

This manual describes the implemented functionality for the SIS3820 output register firmware. Other firmware designs are SIS3820-CLOCK (clock distributor for up to 32 SIS330x VE digitizers), SIS820-LATCH (16 inputs/16 outputs) and SIS3820-SCALER (32 channel multi purpose scaler)

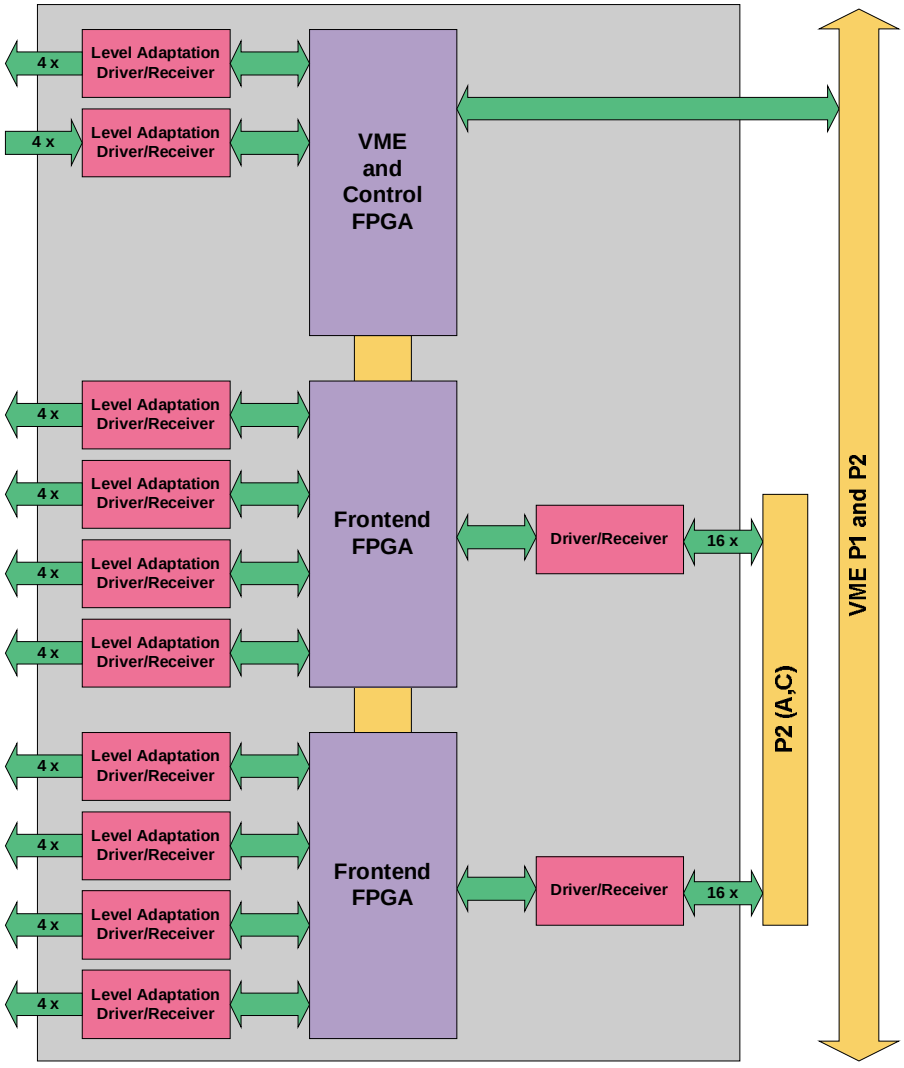
Find below a list of key features of the SIS3820-OutputRegister

- 32 output channels (32 channel option)
- 4 front panel control inputs with scaler
- 4 front panel control outputs with flipflop functionality
- NIM/TTL/ECL/LVDS versions
- flat cable (ECL, TTL and LVDS) and LEMO (TTL/NIM) options
- A16/24/32 D16/32
- Geographical addressing mode (in conjunction with VME64x backplane)
- Interrupt capabilities
- Hot swap (in conjunction with VME64x backplane)
- VME64x Connectors
- VME64x Side Shielding
- VME64x Front panel
- VME64x extractor handles (on request)
- single supply (+5 V)
- in field firmware upgrade capability

4 Functionality

The functionality of the SIS3820 output register is a combination of hardware (printed circuit board) design, stuffing options and firmware. The module consists of two FPGAs that hold the frontend logic and on FPGA that holds the VME interface, the SDRAM controller and the control logic functions. Logic level adaptation is handled by classic DIL components and single inline (SIL) resistor networks. The firmware is loaded from a serial PROM at power up. Both JTAG and VME can be used for in field firmware upgrades/changes.

4.1 Block Diagram



5 Getting started

This section is intended for the first time SIS3820 user. In some cases it may be good enough to use the provided header file and C examples to get acquainted to a couple of the modules functions before looking at the other sections of the manual in more detail. If you have a SIS1100/3100 PCI to VME interface under LINUX or under Win2K/XP with Visual C++ you can use the provided example code without modifications.

5.1 Installation

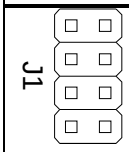
- Select addressing mode with J1 (factory default is A32)
- Select base address with SW1 through SW4 in non geographical addressing (the default base address setting is 0x38000000)
- turn VME crate power off
- install your SIS3820 board in the VME crate
- connect outputs
- turn VME crate power back on
- verify, that the P (power) and R (ready) LEDs are on and all other LEDs are off after the approximately 2s long power up self test cycle

5.1.1.1 Initial VME access test

Both the user LED and readout of the Module Id. and firmware register provide a good way to verify that proper initial communication with the SIS3820 can be established.

6 VME Addressing

The SIS3820 firmware addressing concept is a pragmatic approach to combine standard rotary switch style settings with the use of VME64x backplane geographical addressing functionality.
The base address is defined by the selected addressing mode, which is defined by jumper array J1 and possibly SW4 and SW1 (in non geographical mode).

	Function
	EN_A32
	EN_A24
	EN_GEO
	EN_A16

EN_A32	EN_A24	EN_GEO	EN_A16	Description
x	0	0	0	A32 addressing, address compared withSW4–SW 1
x	0	x	0	A32 addressing, address compared with geographical address
0	x	0	0	A24 addressing, address compared withSW2/SW1
0	0	0	x	A16 addressing, address compared withSW2/SW1
0: jumper open, x: jumper closed				

The tables below illustrates the possible base address settings.

EN A32	EN A24	EN GEO	EN A16	Bits															
				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
x	0	0	0	SW4				SW3				SW2				SW1			
x	0	x	0	0	0	0	GA4	GA3	GA2	GA1	GA0	0				0			
0	x	0	0	y				y				SW2				SW1			
				Bits															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	x	SW2				SW1				A				A			

Shorthand	Explanation
SW1-SW4	Setting of rotary switch SW1 to SW4
y	don't care
GA0-GA4	Geographical address bit as defined by the VME64x(P) backplane
A	Modules address space

Notes:

- This concept allows the use of the SIS3820 in standard VME as well as in VME64x environments, i.e. the user does not have to use a VME64x backplane.
- The factory default setting is 0x38000000 (i.e. SW4=3, SW3=8, EN_A32 closed, EN_GEO, EN_A24 and EN_A16 open/disabled)

6.1 Address map

Offset	R/W	Mode	Function/Register
0x0	R/W	D32	Control/Status register
0x4	R	D32	Module Id. and firmware revision register
0x8	R/W	D32	Interrupt configuration register
0xC	R/W	D32	Interrupt control/status register
0x10	R/W	D32	Direct output data register
0x14	R/W	D32	J/K output data register group 1 Bit 0-15
0x18	R/W	D32	J/K output data register group 2 Bit 15-31
0x30	R	D32	Counter 1
0x34	R	D32	Counter 2
0x38	R	D32	Counter 3
0x3C	R	D32	Counter 4
0x40	W	D32	Clear Counters
0x60	KA	D32	Key reset

7 Register description

The function of the individual registers is described in detail in this section.
The first line after the subsection header (in Courier font) like:

```
#define SIS3820_CONTROL_STATUS      0x0     /* read/write; D32 */
```

7.1 Control/Status Register(0x, write/read)

```
#define SIS3820_CONTROL_STATUS          0x0   /* read/write; D32 */
```

The control register is in charge of the control of some basic properties of the SIS3820 board, like enabling test pulse generators. It is implemented via a selective J/K register, a specific function is enabled by writing a 1 into the set/enable bit, the function is disabled by writing a 1 into the clear/disable bit (which location is 16-bit higher in the register). An undefined toggle status will result from setting both the enable and disable bits for a specific function at the same time.
On read access the same register represents the status register.

Bit	write Function	read Function
31	Clear Invert Control Output 8	0
30	Clear Invert Control Output 7	0
29	Clear Invert Control Output 6	0
28	Clear Invert Control Output 5	0
27	Clear Invert Control Input 4	0
26	Clear Invert Control Input 3	0
25	Clear Invert Control Input 2	0
24	Clear Invert Control Input 1	0
23	Disable control input/Flipflop 4	0
22	Disable control input/Flipflop 3	0
21	Disable control input/Flipflop 2	0
20	Disable control input/Flipflop 1	0
19	Disable reserved 2	0
18	Disable reserved 1	0
17	disable control input counters (*)	0
16	switch off user LED (*)	0
15	Set Invert Control Output 8	Status Set Invert Control Output 8
14	Set Invert Control Output 7	Status Set Invert Control Output 7
13	Set Invert Control Output 6	Status Set Invert Control Output 6
12	Set Invert Control Output 5	Status Set Invert Control Output 5
11	Set Invert Control Input 4	Status Set Invert Control Input 4
10	Set Invert Control Input 3	Status Set Invert Control Input 3
9	Set Invert Control Input 2	Status Set Invert Control Input 2
8	Set Invert Control Input 1	Status Set Invert Control Input 1
7	Enable control input 1/Flipflop 4	Status Enable Flipflop 4
6	Enable control input 1/Flipflop 3	Status Enable Flipflop 3
5	Enable control input 1/Flipflop 2	Status Enable Flipflop 2
4	Enable control input 1/Flipflop 1	Status Enable Flipflop 1
3	Enable reserved 2	0
2	Enable reserved 1	0
1	Enable control input counters	Status input counters (1=on, 0=off)
0	Switch on user LED	Status User LED (1=LED on, 0=LED off)

(*) denotes power up default setting, i.e. the power up reading of the register is 0x0

7.1.1 Enable/disable counter bits

The four counters that are associated with the four control inputs are disabled by default upon power up or key reset. The four enable and disable bits are used to activate and disable all scalers.

7.1.2 Invert/don't invert control input bits

These two groups of 4 bits each allow you to invert the control input for the individual channel to minimize the need for external glue logic.

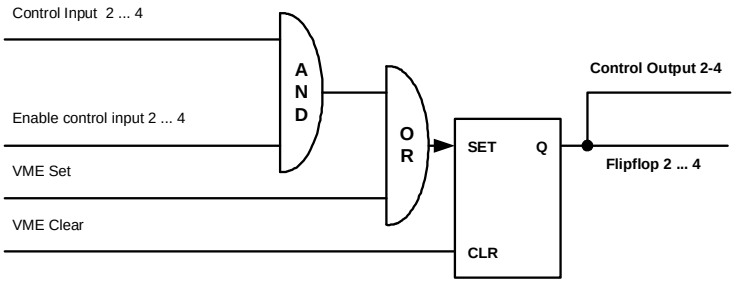
7.1.3 Invert/don't invert control output bits

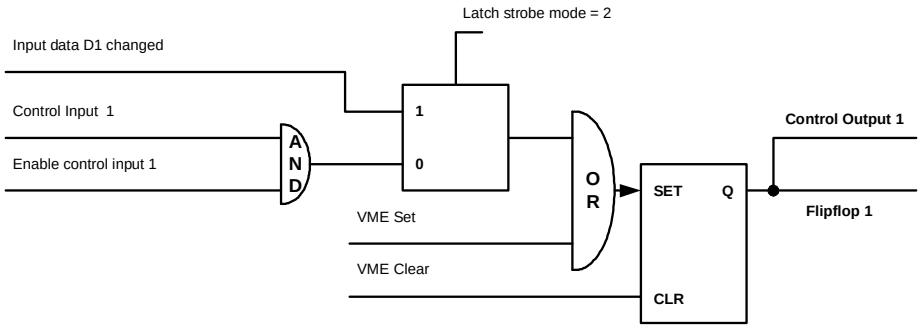
These two groups of 4 bits each allow you to invert the control output for the individual channel to minimize the need for external glue logic. If the flipflop of a channel is used for interaction with deadtime logic you can select between a busy or not busy logic by setting the inversion bit for the corresponding channel.

7.1.4 Flipflop enable

The control outputs of the SIS3820-LATCH can be operated as Flipflops. In Flipflop mode control output N is set with the leading edge of a signal on control input N and reset with the reset Flipflop N bit in the interrupt control register. Flipflop operation for output N is activated by setting the enable Flipflop N bit in the control register. The Flipflop logic is illustrated below.

Note: Flipflop 1 is set by a level change of input data bit 1 (LSB) if bit 3 of the control register is set to 1 (latch strobe condition bit change). This feature can be used to one or several frontend crates by incrementing a up to 16-bit wide event number with the output section of another SIS3820-LATCH (or a SIS3610 in event number increment mode) in a "master crate".





7.2 Module Id. and Firmware Revision Register (0x4, read)

```
#define SIS3820_MODID                    0x4   /* read only; D32 */
```

This register reflects the module identification of the SIS3820 and its minor and major firmware revision levels. The major revision level will be used to distinguish between substantial design differences and experiment specific designs, while the minor revision level will be used to mark user specific adaptations.

Bit	Function	Reading
31	Module Id. Bit 15	3
30	Module Id. Bit 14	
29	Module Id. Bit 13	
28	Module Id. Bit 12	
27	Module Id. Bit 11	8
26	Module Id. Bit 10	
25	Module Id. Bit 9	
24	Module Id. Bit 8	
23	Module Id. Bit 7	2
22	Module Id. Bit 6	
21	Module Id. Bit 5	
20	Module Id. Bit 4	
19	Module Id. Bit 3	0
18	Module Id. Bit 2	
17	Module Id. Bit 1	
16	Module Id. Bit 0	
15	Major Revision Bit 7	
14	Major Revision Bit 6	
13	Major Revision Bit 5	
12	Major Revision Bit 4	
11	Major Revision Bit 3	
10	Major Revision Bit 2	
9	Major Revision Bit 1	
8	Major Revision Bit 0	
7	Minor Revision Bit 7	
6	Minor Revision Bit 6	
5	Minor Revision Bit 5	
4	Minor Revision Bit 4	
3	Minor Revision Bit 3	
2	Minor Revision Bit 2	
1	Minor Revision Bit 1	
0	Minor Revision Bit 0	

7.2.1 Major and minor revision numbers

Refer to http://www.struck.de/sis3820firm.htm for revision numbers used to date
The major revision for the 32 bit output register is 0xF3, so the reding of the register for the initial x01 minor revision is 0x3820F301.

7.3 Interrupt configuration register (0x8)

```
#define SIS3820_IRQ_CONFIG                0x8   /* read/write; D32 */
```

In conjunction with the interrupt control register this read/write register controls the VME interrupt behaviour of the SIS3820-LATCH. Four interrupt sources are implemented, they are associated with the four control inputs.
The interrupter type is DO8 .

7.3.1 IRQ mode

In RORA (release on register access) mode the interrupt will be pending until the IRQ source is cleared by specific access to the corresponding disable VME IRQ source bit. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again.
In ROAK (release on acknowledge) mode , the interrupt condition will be cleared (and the IRQ source disabled) as soon as the interrupt is acknowledged by the CPU. After the interrupt is serviced the source has to be activated with the enable VME IRQ source bit again. ROAK IRQ mode can be used in conjunction with the University of Bonn LINUX Tundra Universe II driver by Dr. Jürgen Hannappel on Intel based VME SBCs.

Bit	Function	Default
31		0
...		0
16		0
15		0
14		0
13		0
12	RORA/ROAK Mode (0: RORA; 1: ROAK)	0
11	VME IRQ Enable (0=IRQ disabled, 1=IRQ enabled)	0
10	VME IRQ Level Bit 2	0
9	VME IRQ Level Bit 1	0
8	VME IRQ Level Bit 0	0
7	IRQ Vector Bit 7; placed on D7 during VME IRQ ACK cycle	0
6	IRQ Vector Bit 6; placed on D6 during VME IRQ ACK cycle	0
5	IRQ Vector Bit 5; placed on D5 during VME IRQ ACK cycle	0
4	IRQ Vector Bit 4; placed on D4 during VME IRQ ACK cycle	0
3	IRQ Vector Bit 3; write with 0, read back status of input 4 during VME IRQ ACK cycle	0
2	IRQ Vector Bit 2; write with 0, read back status of input 3 during VME IRQ ACK cycle	0
1	IRQ Vector Bit 1; write with 0, read back status of input 2 during VME IRQ ACK cycle	0
0	IRQ Vector Bit 0; write with 0, read back status of input 1 during VME IRQ ACK cycle	0

The power up default value reads 0x 00000000

Note: Bits 0 to 3 will return a 0 during a standard VME read access

7.4 Interrupt Control/Status register (0xC)

```
#define SIS3820_IRQ_CONTROL              0xC   /* read/write; D32 */
```

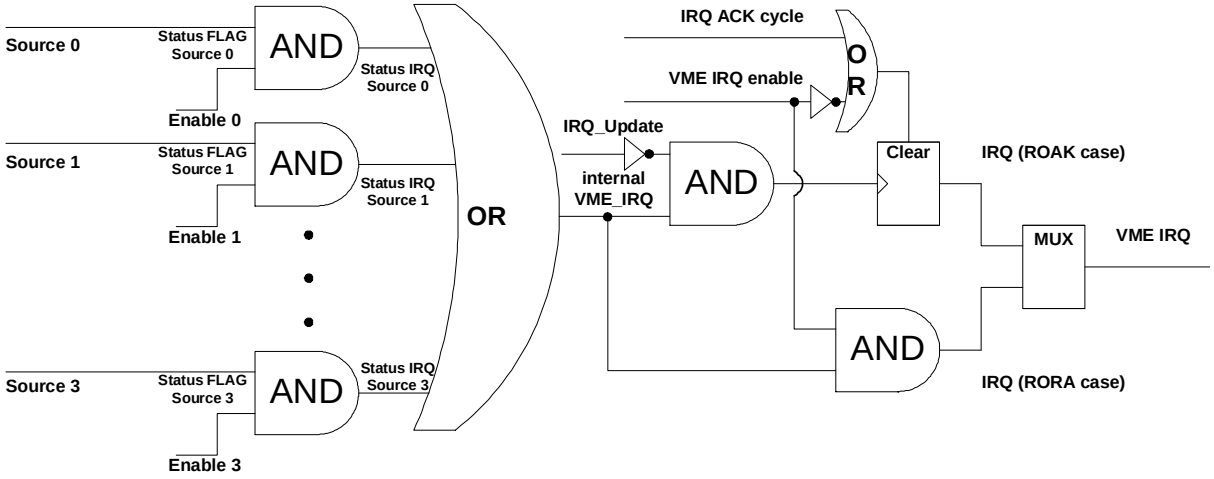
The interrupt sources are enabled with the interrupt control register. The interrupt source is cleared in the interrupt service routine. The status internal IRQ flag can be used for tests without activating VME interrupt generation. It is set whenever an interrupt would be generated if interrupting would be enabled in the interrupt configuration register.
fourth condition is reserved for future use.

Bit	Function (w)	(r)	Default
31	1 Shot : IRQ_UPDATE	0	0
30	unused	0	0
29	unused	0	0
	unused	0	0
27	Set IRQ source 3	Status IRQ source 3 (FlipFlop 4)	0
26	Set IRQ source 2	Status IRQ source 2 (FlipFlop 3)	0
25	Set IRQ source 1	Status IRQ source 1 (FlipFlop 2)	0
24	Set IRQ source 0	Status IRQ source 0 (FlipFlop 1)	0
23	unused	0	0
22	unused	0	0
21	unused	0	0
20	unused	0	0
19	Clear IRQ source 3/reset Flipflop 4	Status flag source 3 (Flipflop 4)	0
18	Clear IRQ source 2/reset Flipflop 3	Status flag source 2 (Flipflop 3)	0
17	Clear IRQ source 1/reset Flipflop 2	Status flag source 1 (Flipflop 2)	0
16	Clear IRQ source 0/reset Flipflop 1	Status flag source 0 (Flipflop 1)	0
15	unused	Status VME IRQ	0
14	unused	Status internal IRQ	0
13	unused	0	0
12	unused	0	0
11	Disable IRQ source 3	0	0
10	Disable IRQ source 2	0	0
9	Disable IRQ source 1	0	0
8	Disable IRQ source 0	0	0
7	unused	0	0
6	unused	0	
5	unused	0	0
4	unused	0	0
3	Enable IRQ source 3	Status enable source 3 (read as 1 if enabled, 0 if disabled)	0
2	Enable IRQ source 2	Status enable source 2 (read as 1 if enabled, 0 if disabled)	0
1	Enable IRQ source 1	Status enable source 1 (read as 1 if enabled, 0 if disabled)	0
0	Enable IRQ source 0	Status enable source 0 (read as 1 if enabled, 0 if disabled)	0

The power up default value reads 0x 00000000

Note: The clear IRQ source bits are relevant for edge sensitive IRQs only

The generation of the status flags, the IRQ flags and the actual IRQ is illustrated with the schematic below:



7.5 Output data registers (0x10 and 0x14/0x18)

The output levels of the 16 outputs can be controlled by three registers

- direct output data register (read/write)
- J/K output registers group 1 and 2 (write only)

The level will be set according to the last transaction to both registers and can be read back from the direct output data register (even if it was altered by the J/K output register). While it is most straightforward to define a complete pattern like an event number with the direct output data register, the J/K register can be used to set/clear or flip an individual bit only without the hassle to remember the previous state.

7.5.1 Direct output data register (0x10)

```
#define SIS3820_DATA_D_OUT                0x10  /* read/write; D32 */
```

This read/write register defines the data which are applied to the output drivers.

Bit	Function
31	Output Bit 31
...	...
16	Output Bit 16
15	Output Bit 15
14	Output Bit 14
13	Output Bit 13
12	Output Bit 12
11	Output Bit 11
10	Output Bit 10
9	Output Bit 9
8	Output Bit 8
7	Output Bit 7
6	Output Bit 6
5	Output Bit 5
4	Output Bit 4
3	Output Bit 3
2	Output Bit 2
1	Output Bit 1
0	Output Bit 0

The default state upon power up and key reset is 0x0, i.e. all outputs at 0

7.5.2 J/K output data register group 1 (0x14)

```
#define SIS3820_DATA_JK_OUT              0x14  /* read/write; D32 */
#define SIS3820_DATA_JK_OUT1             0x14  /* read/write; D32 */
```

The second way to control the output level of the SIS3820 output register is access to this write only register. It is implemented in a J/K fashion. Writing a 1 to the set bit (bits 0-15) will set the corresponding bit will result in a logic 1 on the output. Writing a 1 to the clear bit (bits 16-31) will clear the output level. Priority is on set if both set and clear are 1 at the same time.
The current output pattern can be read back from the direct output register .

Bit	Function
31	Clear Output Bit 15
30	Clear Output Bit 14
29	Clear Output Bit 13
28	Clear Output Bit 12
27	Clear Output Bit 11
26	Clear Output Bit 10
25	Clear Output Bit 9
24	Clear Output Bit 8
23	Clear Output Bit 7
22	Clear Output Bit 6
21	Clear Output Bit 5
20	Clear Output Bit 4
19	Clear Output Bit 3
18	Clear Output Bit 2
17	Clear Output Bit 1
16	Clear Output Bit 0
15	Set Output Bit 15
14	Set Output Bit 14
13	Set Output Bit 13
12	Set Output Bit 12
11	Set Output Bit 11
10	Set Output Bit 10
9	Set Output Bit 9
8	Set Output Bit 8
7	Set Output Bit 7
6	Set Output Bit 6
5	Set Output Bit 5
4	Set Output Bit 4
3	Set Output Bit 3
2	Set Output Bit 2
1	Set Output Bit 1
0	Set Output Bit 0

7.5.3 J/K output data register group 2 (0x18)

```
#define SIS3820_DATA_JK_OUT2              0x18  /* read/write; D32 */
```

Same function as J/K output data register group 2 but for bits 16-31

Bit	Function
31	Clear Output Bit 31
30	Clear Output Bit 30
29	Clear Output Bit 29
28	Clear Output Bit 28
27	Clear Output Bit 27
26	Clear Output Bit 26
25	Clear Output Bit 25
24	Clear Output Bit 24
23	Clear Output Bit 23
22	Clear Output Bit 22
21	Clear Output Bit 21
20	Clear Output Bit 20
19	Clear Output Bit 19
18	Clear Output Bit 18
17	Clear Output Bit 17
16	Clear Output Bit 16
15	Set Output Bit 31
14	Set Output Bit 30
13	Set Output Bit 29
12	Set Output Bit 28
11	Set Output Bit 27
10	Set Output Bit 26
9	Set Output Bit 25
8	Set Output Bit 24
7	Set Output Bit 23
6	Set Output Bit 22
5	Set Output Bit 21
4	Set Output Bit 20
3	Set Output Bit 19
2	Set Output Bit 18
1	Set Output Bit 17
0	Set Output Bit 16

7.6 Counter registers 0x30,0x34, 0x38, 0x3C

```
#define SIS3820_LATCH_COUNTER1                  0x30 /* read only; D32 */
#define SIS3820_LATCH_COUNTER2                  0x34 /* read only; D32 */
#define SIS3820_LATCH_COUNTER3                  0x38 /* read only; D32 */
#define SIS3820_LATCH_COUNTER4                  0x3C /* read only; D32 */
```

This set of 4 32-bit registers hold the (200 MHz) scalers which can be used to count signals on the individual control input channels.

Address	Contents
0x3C	Counter 4
0x38	Counter 3
0x34	Counter 2
0x30	Counter 1

7.7 Clear counter register 0x40

```
#define SIS3820_LATCH_COUNTER_CLEAR             0x40 /* write only; D32 */
```

This write only register is used to clear an arbitrary combination of counters.

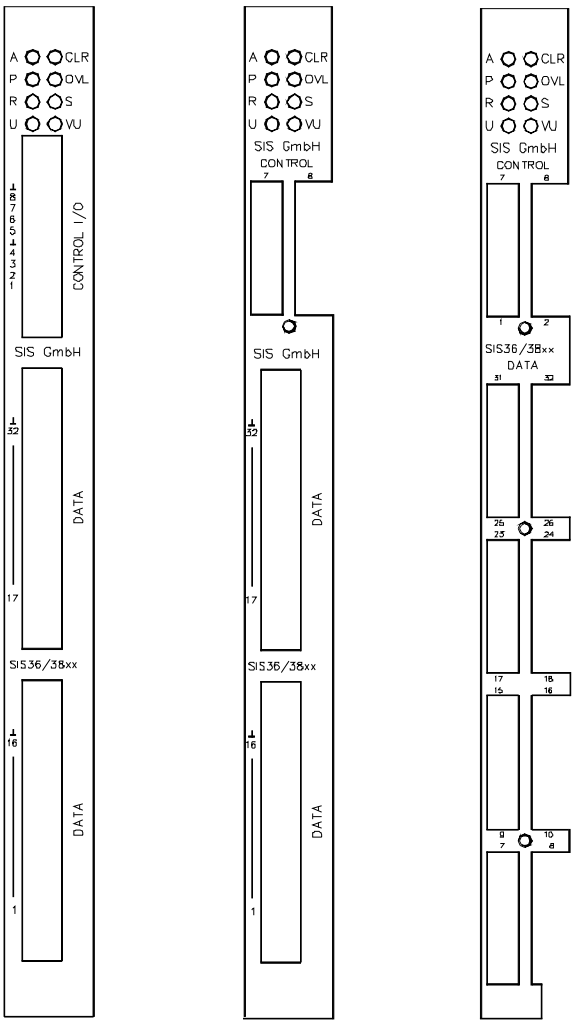
Bit	Function
31	Unused
...	...
4	Unused
3	1: Clear counter 4, 0: don’t care
2	1: Clear counter 3, 0: don’t care
1	1: Clear counter 2, 0: don’t care
0	1: Clear counter 1, 0: don’t care

8 Front panel elements

8.1 Front Panel Layout

The front panel of the SIS3820 is equipped with 8 LEDs, 8 control in- and outputs and 32 frontend in/outputs. On flat cable units (ECL and TTL) the control connector is a 20 pin header flat cable connector and the channel inputs are fed via two 34-pin headers. On LEMO (NIM and TTL) units the control in- and outputs are grouped to one 8 channel block and the counter inputs are grouped into 2 blocks of 16 channels. A mixed LEMO control/flat cable counter input version is available also. The units are 4 TE (one VME slot) wide, the front panel is of EMC shielding type. VIPA extractor handles are available on request or can be retrofitted by the user, if he wants to change to a VIPA crate at a later point in time.
In the drawing below you can find the flat cable (left hand side), the LEMO control/flat cable input (middle) and LEMO front panel layouts.

Note: Only the aluminium portion without the extractor handle mounting fixtures is shown

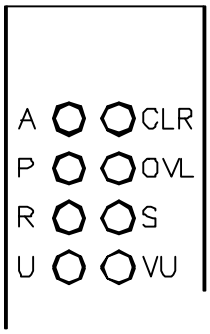


8.2 Front Panel LEDs

The SIS3820 has 8 front panel LEDs to visualize part of the units status. Three LEDs according to the VME64xP standard (Power, Access and Ready) plus 5 additional LEDs (VME user LED, Clear, Overflow, Scaler enable and VIPA user LED).

Designation	LED	Color	Function
A	Access	yellow	Signals VME access to the unit
P	Power	red	Flags presence of VME power
R	Ready	green	Signals configured logic
U	VME user LED	green	To be switched on/off under user program control
CLR	Clear	yellow	Status Flipflop 4
OVL	Overflow	red	Status Flipflop 3
S	Scaler Enable	green	Status Flipflop 2
VU	VIPA user LED	green	Status Flipflop 1

The LED locations are shown in the portion of the front panel drawing below.



The VME Access, Clear and Scaler enable LEDs are monostable (i.e. the duration of the on phase is stretched for better visibility), the other LEDs reflect the current status.
An LED test cycle is performed upon power up (refer to the chapter 12.6).

8.3 Flat cable Input/Output Pin Assignments

8.3.1 ECL

Data-Connector Channel 1-16

PIN	SIGNAL	SIGNAL	PIN
32	IN16 -	IN16 +	31
30	IN15 -	IN15 +	29
28	IN14 -	IN14+	27
26	IN13 -	IN13 +	25
24	IN12 -	IN12 +	23
22	IN11 -	IN11 +	21
20	IN10 -	IN10 +	19
18	IN9 -	IN9 +	17
16	IN8 -	IN8 +	15
14	IN7 -	IN7 +	13
12	IN6 -	IN6 +	11
10	IN5 -	IN5 +	9
8	IN4 -	IN4 +	7
6	IN3 -	IN3 +	5
4	IN2 -	IN2 +	3
2	IN1 -	IN1 +	1

Front view

INx + = ECL High active
INx - = ECL Low active

Data-Connector Channel 17-32

PIN	SIGNAL	SIGNAL	PIN
32	IN32 -	IN32 +	31
30	IN31 -	IN31 +	29
28	IN30 -	IN30 +	27
26	IN29 -	IN29 +	25
24	IN28 -	IN28 +	23
22	IN27 -	IN27 +	21
20	IN26 -	IN26 +	19
18	IN25 -	IN25 +	17
16	IN24 -	IN24 +	15
14	IN23 -	IN23 +	13
12	IN22 -	IN22 +	11
10	IN21 -	IN21 +	9
8	IN20 -	IN20 +	7
6	IN19 -	IN19 +	5
4	IN18 -	IN18 +	3
2	IN17 -	IN17 +	1

Front view

INx + = ECL High active
INx - = ECL Low active

Control-Connector Input 1-4 /Output 5-8

PIN	SIGNAL	SIGNAL	PIN
20	GND	GND	19
18	OUT8-	OUT8+	17
16	OUT7-	OUT7+	15
14	OUT6-	OUT6+	13
12	OUT5-	OUT5+	11
10	GND	GND	9
8	IN4 -	IN4 +	7
6	IN3 -	IN3 +	5
4	IN2 -	IN2 +	3
2	IN1 -	IN1 +	1

Front view

INx + = ECL High active
INx - = ECL Low active

OUTx + = ECL High active
OUTx - = ECL Low active

8.3.2 TTL

Data-Connector Channel 1-16

PIN	SIGNAL	SIGNAL	PIN
32	IN16 -	GND	31
30	IN15 -	GND	29
28	IN14 -	GND	27
26	IN13 -	GND	25
24	IN12 -	GND	23
22	IN11 -	GND	21
20	IN10 -	GND	19
18	IN9 -	GND	17
16	IN8 -	GND	15
14	IN7 -	GND	13
12	IN6 -	GND	11
10	IN5 -	GND	9
8	IN4 -	GND	7
6	IN3 -	GND	5
4	IN2 -	GND	3
2	IN1 -	GND	1

Front view

INx - = TTL Low active (74F245)

Data-Connector Channel 17-32

PIN	SIGNAL	SIGNAL	PIN
32	IN32 -	GND	31
30	IN31 -	GND	29
28	IN30 -	GND	27
26	IN29 -	GND	25
24	IN28 -	GND	23
22	IN27 -	GND	21
20	IN26 -	GND	19
18	IN25 -	GND	17
16	IN24 -	GND	15
14	IN23 -	GND	13
12	IN22 -	GND	11
10	IN21 -	GND	9
8	IN20 -	GND	7
6	IN19 -	GND	5
4	IN18 -	GND	3
2	IN17 -	GND	1

Front view

INx - = TTL Low active (74F245)

Control-Connector Input 1-4 /Output 5-8

PIN	SIGNAL	SIGNAL	PIN
20	GND	GND	19
18	OUT8-	GND	17
16	OUT7-	GND	15
14	OUT6-	GND	13
12	OUT5-	GND	11
10	GND	GND	9
8	IN4 -	GND	7
6	IN3 -	GND	5
4	IN2 -	GND	3
2	IN1 -	GND	1

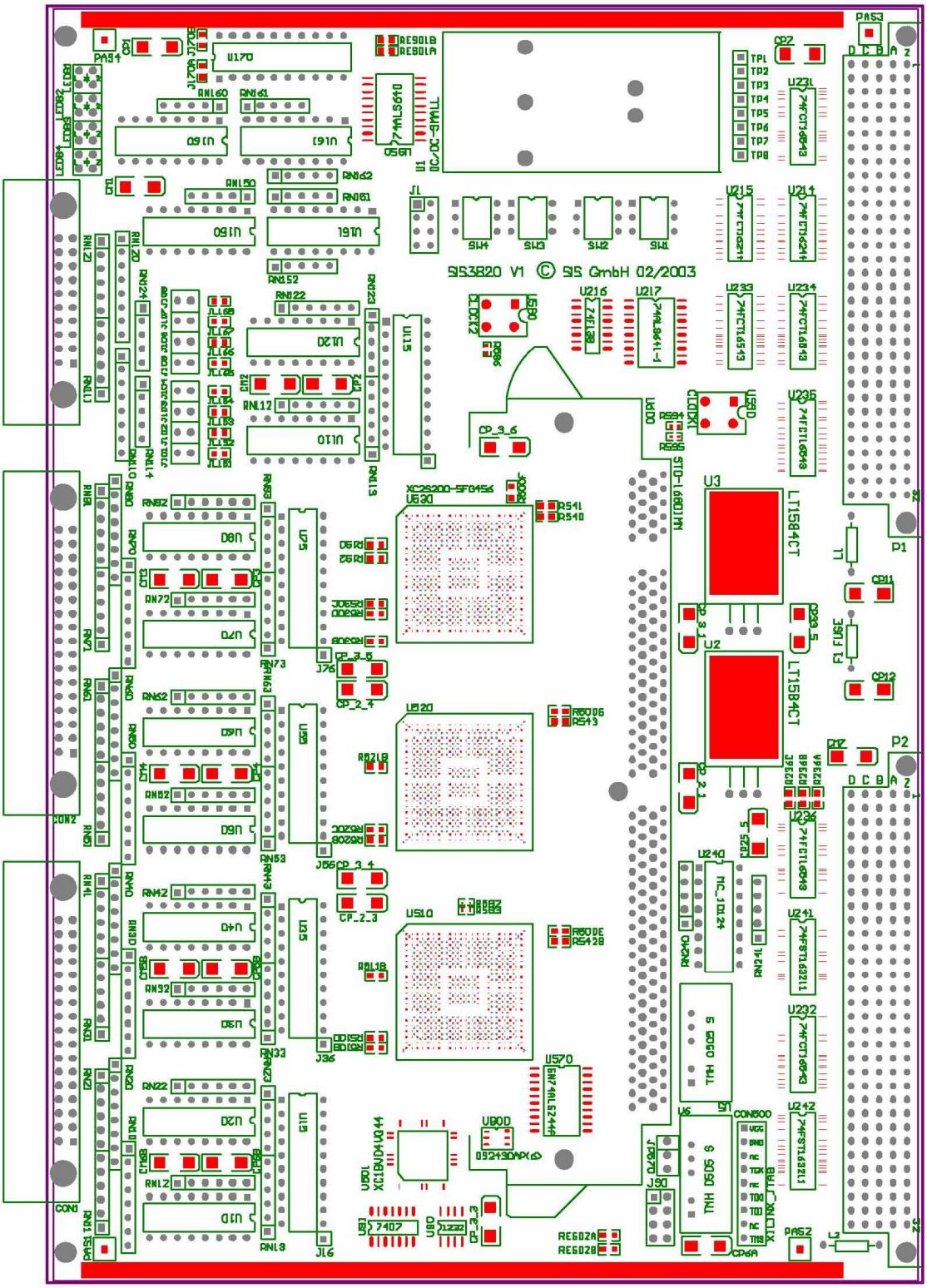
Front view

INx - = TTL Low active (74F245)

OUTx - = TTL Low active (74F244)

9 Board Layout

Find below a printout of the top assembly drawing.



10 Jumper settings/pinouts

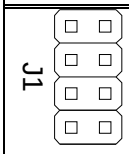
The SIS3820 has 3 jumper fields and a JTAG connector.

Jumper field	Function
J1	VME addressing mode
J90	Reset behavior
JP570	JTAG source
CON500	JTAG connector

The first pin of the jumper fields is marked by a square pin on the solder side and an extra frame on the silk screen of the component side.

10.1 J1

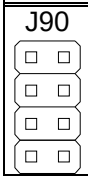
J1 is in charge of the VME addressing mode. The user can select between rotary switch selected A32, A24 and A16 addressing and geographical A32 addressing.. . . A closed position selects the corresponding function.

	Function
	EN_A32
	EN_A24
	EN_GEO
	EN_A16

The default setting is EN_A32 closed and all other positions opened.

10.2 J90

J90 controls the reset behavior of the SIS3820.

	Function
	reserved
	connect VME reset to SIS3820 reset
	reserved
	enable watchdog

The default setting is VME reset and enable watchdog closed and all other positions opened.

Note: open the enable watchdog for firmware upgrades

10.3 JP570 JTAG source

Firmware can be loaded to the XC18V04 serial PROM via a JTAG download cable (XILINX JTAG-PC4 e.g.) or via the VME interface of the SIS3830. Please note, that errors during this process can render a module temporarily in non working condition.. JP570 has 3 pins. Depending on whether pins 1 and 2 or 2 and 3 are closed the JTAG source is defined as listed below.

Closed	JTAG source
1-2	JTAG connector CON 500
2-3	VME

10.4 CON500 JTAG

The SIS3820 on board logic can load its firmware from a serial PROMs . The firmware can be upgraded through VME (future option) or the JTAG connector. A list of firmware designs can be found under http://www.struck.de/sis3820firm.htm.
Hardware like the XILINX HW-JTAG-PC in connection with the appropriate software (the XILINX WebPACK is furnished on the accompanying CDROM) will be required for in field JTAG firmware upgrades through the JTAG connector.
The JTAG connector is a 9 pin single row 1/10 inch header, the pin assignment on the connector can be found in the table below.

Pin	Short hand	Description
1	VCC	Supply voltage
2	GND	Ground
3	nc	not connected, cut to avoid polarity mismatch
4	TCK	test clock
5	nc	not connected
6	TDO	test data out
7	TDI	test data in
8	nc	not connected
9	TMS	test modus

Note: close the J90 disable watchdog jumper for firmware upgrades

11 Input Configuration

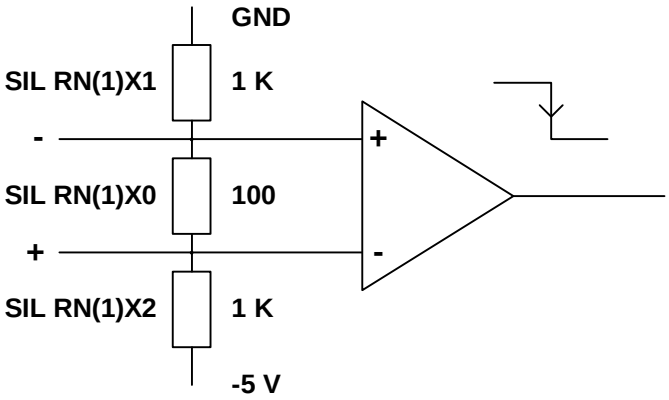
SIS36/38xx boards are available for NIM, TTL , ECL and LVDS input levels and in LEMO and flat cable versions. The boards are factory configured for the specified input level and connector type. Input termination is installed.

11.1 ECL

The 100 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels	1 K Networks
RN10	1-4	RN11/12
RN20	5-8	RN21/22
RN30	9-12	RN31/32
RN40	13-16	RN41/41
RN50	17-20	RN51/52
RN60	21-24	RN61/62
RN70	25-28	RN71/72
RN80	29-32	RN81/82
RN110	Control 1-4	RN111/RN112
RN120	Control 5-8	RN121/RN122

The schematics of the ECL input circuitry is shown below.

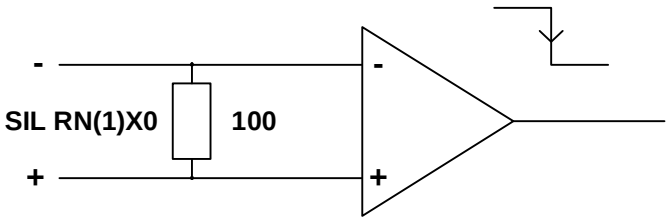


11.2 LVDS

The 100 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels
RN10	1-4
RN20	5-8
RN30	9-12
RN40	13-16
RN50	17-20
RN60	21-24
RN70	25-28
RN80	29-32
RN110	Control 1-4
RN120	Control 5-8

The schematics of the LVDS input circuitry is shown below.

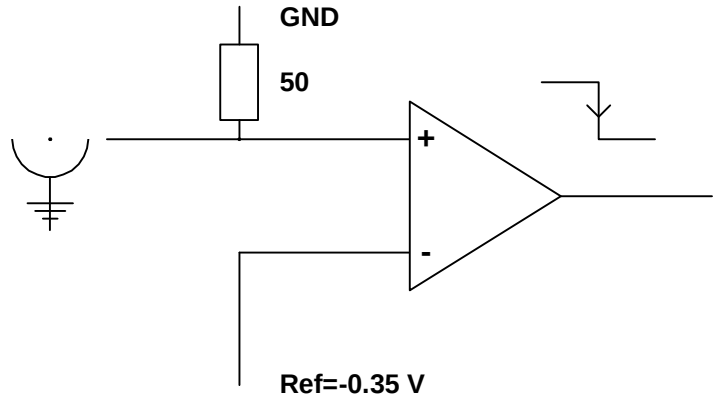


11.3 NIM

The 50 Ω input termination can be removed in groups of four channels by removing the corresponding resistor networks. The termination of single control inputs can be disabled with jumpers J101 through J108, an open jumper disables the termination of the corresponding channel.

Network	Channels
U15 (Pins 10 to 6)	1-4
U15 (Pins 1 to 5)	5-8
U35 (Pins 10 to 6)	9-12
U35(Pins 1 to 5)	13-16
U55 (Pins 10 to 6)	17-20
U55 (Pins 1 to 5)	21-24
U75 (Pins 10 to 6)	25-28
U75 (Pins 1 to 5)	29-32
U115 (Pins 10 to 6)	Control 1-4
U115 (Pins 1 to 5)	Control 5-8

The schematics of the NIM input circuitry is shown below.

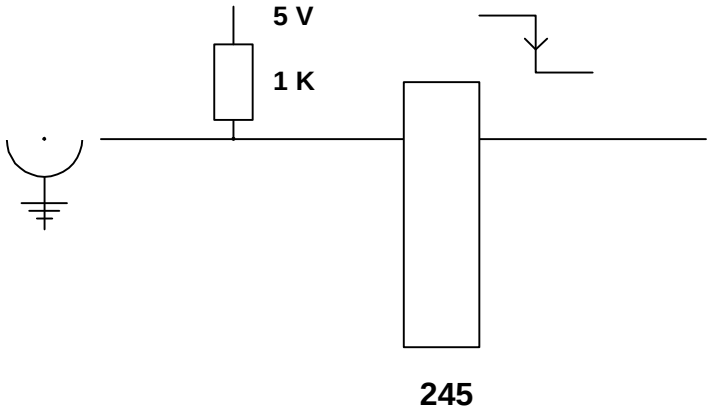


11.4 TTL

The TTL input level option is possible with LEMO and flat cable connectors.

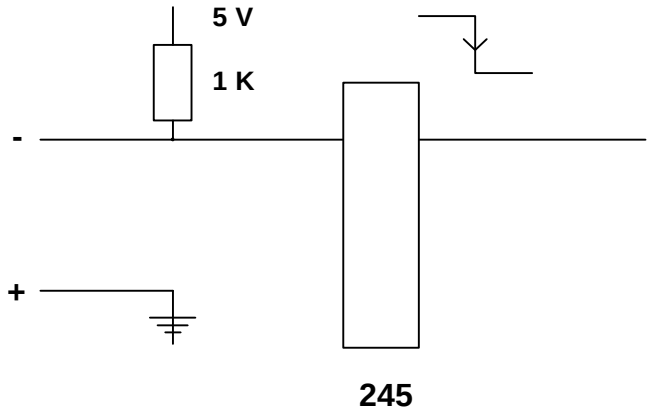
11.4.1 TTL/LEMO

The (low active) TTL/LEMO input circuitry is sketched below. A high active version can be implemented by replacing the 74F245 with a 74F640



11.4.2 TTL/Flat Cable

In the flat cable TTL version the positive (right hand side) of the connector is tied to ground.



12 Appendix

12.1 P2 row A/C pin assignments

The P2 connector of the SIS3820 (in 64 channel or clock module configuration) has connections on rows A and C to feed the second set of 32 inputs to the module or for operation as backplane clock distributor for the SIS330x digitizer family. This implies, that the module can not be operated in a VME slot with a special A/C backplane, like VSB e.g.. The pin assignments of P2 rows A/C of the SIS3820 for both scaler and clock module is shown below. 32 channel versions do not make use of P2 rows A/C.

P2A	Scaler Function	Clock Function	P2C	Scaler Function	Clock Function
1	not connected	-5.2 V	1	not connected	-5.2 V
2	not connected	-5.2 V	2	not connected	-5.2 V
3	not connected	-5.2 V	3	not connected	-5.2 V
4	not connected	not connected	4	not connected	not connected
5	not connected	not connected	5	not connected	not connected
6	DGND	DGND	6	DGND	DGND
7	Control 1	P2_CLOCK_H	7	Control 0	P2_CLOCK_L
8	DGND	DGND	8	DGND	DGND
9	Control 3	P2_START_H	9	Control 2	P2_START_L
10	Control 5	P2_STOP_H	10	Control 4	P2_STOP_L
11	Control 7	P2_TEST_H	11	Control 6	P2_TEST_L
12	DGND	DGND	12	DGND	DGND
13	DGND	DGND	13	DGND	DGND
14	G34_L16	not connected	14	G34_L15	not connected
15	G34_L14	not connected	15	G34_L13	not connected
16	G34_L12	not connected	16	G34_L12	not connected
17	G34_L10	not connected	17	G34_L9	not connected
18	G34_L8	not connected	18	G34_L7	not connected
19	G34_L6	not connected	19	G34_L5	not connected
20	G34_L4	not connected	20	G34_L3	not connected
21	G34_L2	not connected	21	G34_L1	not connected
22	DGND	DGND	22	DGND	DGND
23	G12_L16	not connected	23	G12_L15	not connected
24	G12_L14	not connected	24	G12_L13	not connected
25	G12_L12	not connected	25	G12_L11	not connected
26	G12_L10	not connected	26	G12_L9	not connected
27	G12_L8	not connected	27	G12_L7	not connected
28	G12_L6	not connected	28	G12_L5	not connected
29	G12_L4	not connected	29	G12_L3	not connected
30	G12_L2	not connected	30	G12_L1	not connected
31	DGND	DGND	31	DGND	DGND
32	not connected	not connected	32	not connected	not connected

12.2 Row d and z Pin Assignments

The SIS3820 is ready for the use with VME64x and VME64xP backplanes. Features include geographical addressing (PCB revisions V2 and higher) and live insertion (hot swap). The used pins on the d and z rows of the P1 and P2 connectors are listed below.

Position	P1/J1		P2/J2	
	Row z	Row d	Row z	Row d
1		VPC (1)		
2	GND	GND (1)	GND	
3				
4	GND		GND	
5				
6	GND		GND	
7				
8	GND		GND	
9		GAP*		
10	GND	GA0*	GND	
11	RESP*	GA1*		
12	GND		GND	
13		GA2*		
14	GND		GND	
15		GA3*		
16	GND		GND	
17		GA4*		
18	GND		GND	
19				
20	GND		GND	
21				
22	GND		GND	
23				
24	GND		GND	
25				
26	GND		GND	
27				
28	GND		GND	
29				
30	GND		GND	
31		GND (1)		GND (1)
32	GND	VPC (1)	GND	VPC (1)

Note: Pins designated with (1) are so called MFBL (mate first-break last) pins on the installed 160 pin connectors, VPC(1) pins are connected via inductors.

12.3 Connector Types

Find below a list of connector types that are used on the SIS3820.

Connector	Purpose	Part Number
160 pin zabcd	VME P1/P2	Harting 02 01 160 2101
20 pin header	Control (flat cable versions)	DIN41651 20 Pin (AMP e.g.)
34 pin header	Inputs (flat cable versions)	DIN41651 34 Pin (AMP e.g.)
LEMO	Control and Input (LEMO versions)	LEMO ERN.00.250.CTL
SDRAM	SDRAM memory socket	Berg 88638-60002

12.4 Power consumption

The SIS3820 is a single +5 V supply board. Lower positive voltages (3.3 V and 2.5 V) are generated with low dropout regulators. –5 V is generated with up to 3 DC/DC converters.

Board type	Voltage	Current
SIS3820-SCALER (32 ECL channels)	5 V	2,0 A
SIS3820-SCALER (32 TTL channels	5 V	1,3 A
SIS3820-CLOCK (32 NIM channels)	5 V	3,2 A

12.5 Operating conditions

12.5.1 Cooling

Although the SIS3820 output register is mainly a 2.5 and 3.3 V low power design, forced air flow is required for the operation of the board. The board may be operated in a non condensing environment at ambient temperatures between 10° and 40° Celsius.

12.5.2 Hot swap/live insertion

Please note, that the VME standard does not support hot swap by default. The SIS3820 is configured for hot swap in conjunction with a VME64x backplane. In non VME64x backplane environments the crate has to be powered down for module insertion and removal.

12.6 LED (selftest)

During power up self test and FPGA configuration all LEDs except the Ready (R) LED are on. After the initialization phase is completed, all LEDs except the Ready (R) LED and the Power (P) have to go off. Differing behavior indicates either a problem with the download of the firmware boot file or one or more FPGAs and/or the download logic.

13 Index

A16 28
A24 6, 28
A32 6, 28
address map 10
addressing
  geographical 6
backplane 6, 9, 36
block diagram 7
board layout 27
Bonn 16
CON500 29
connector 6
Connector Types 36
cooling 36
counter
  disable 13
  enable 13
D16 6
D32 6
DC/DC 36
DO8 16
ECL 25, 30
EN_A16 9
EN_A24 9
EN_A32 9
EN_GEO 9
firmware 29
flipflop 24
  enable 14
FPGA 36
front panel 6
Front Panel
  LED 24
Front Panel Layout 23
GA 9
geographical addressing 35
GND 29
hot swap 35, 36
Input Configuration 30
installation 8
Intel 16
interrupter mode 16
interrupter type 16
introduction 5
invert
  control input 13
  control output 13
IRQ
  Flipflop 1 17
  Flipflop 2 17
  Flipflop 3 17
  Flipflop 4 17
IRQ mode 16
  ROAK 16
  RORA 16
J/K 20
J1 9
J90 29
JP570 29
JTAG 7, 29
jumper settings 28
LED 24
  Access 24
  Color 24
  power 36
  Power 24
  ready 36
  Ready 24
  selftest 36
  user 12
LEMO 36
LINUX 16
live insertion 35, 36
LVDS 31
monostable 24
NIM 32
operating conditions 36
P1 35
P2 35
  pin assignments 34
PCB 35
Pin Assignments 25
pin header 36
power consumption 36
PROM 7, 29
register
  clear counter 22
  control 15
  direct output 20
  firmware revision 15
  interrupt configuration 16
  interrupt control 14, 16
  interrupt control/status 17
  J/K output 20
  latched input data 22
  module Id. 15
  output data 19
  output data group 1 20
  output data group 2 21
ROAK 16
RORA 16
rotary switch 9
SBC 16
SDRAM 7, 36
side cover 6
SIL 7
SIS1100/3100 8
SW1 8, 9
SW2 9
SW3 9
SW4 8, 9
TCK 29
TDI 29
TDO 29

Technical Properties/Features 6
termination 30, 31
TMS 29
TTL 26, 33
Tundra 16
Universe II 16
user
LED 12
VCC 29
VME 36
access test 8
P1 36
P2 36
VME addressing 9
VME64x 6, 9, 35, 36
VME64xP 35
VSB 34
watchdog 28
XC18V04 29