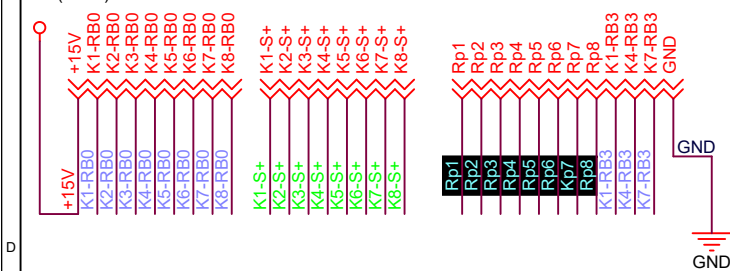
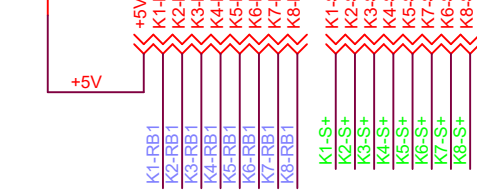


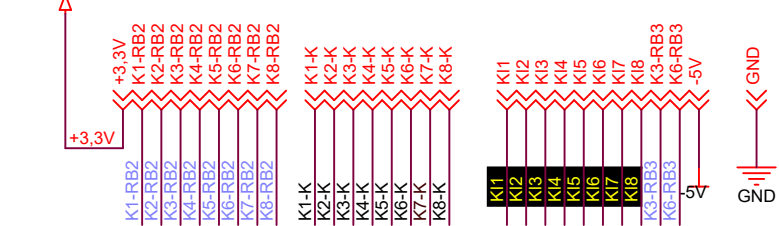
VCC(+15V)



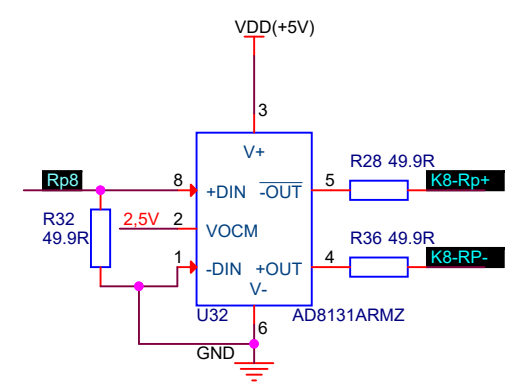
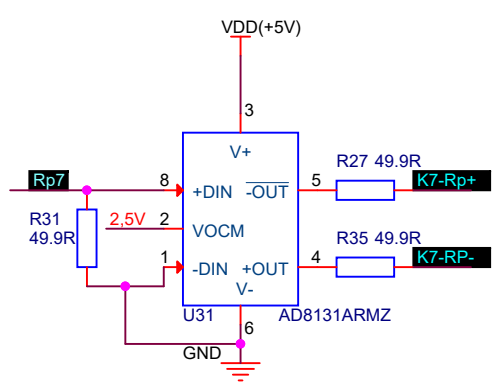
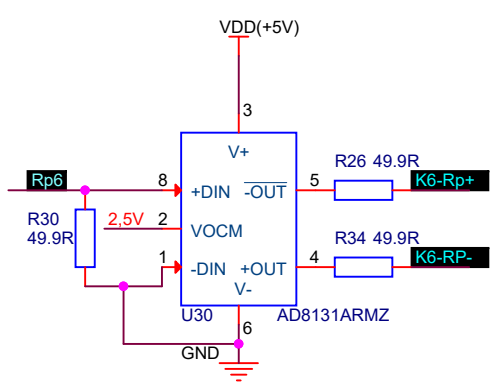
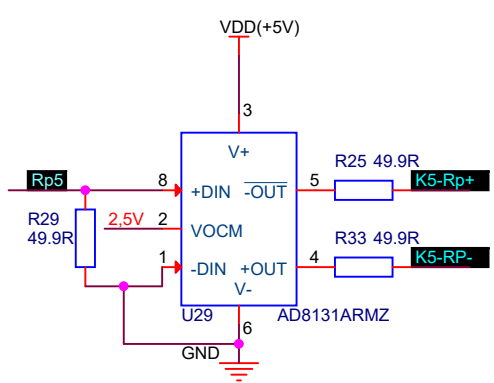
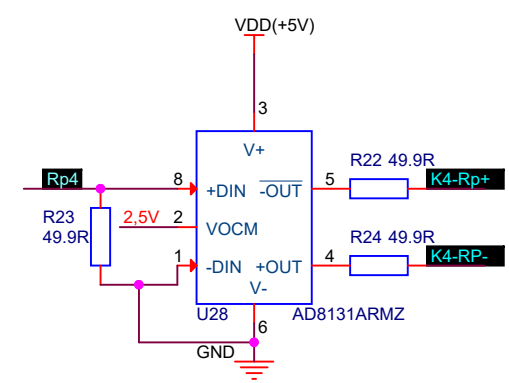
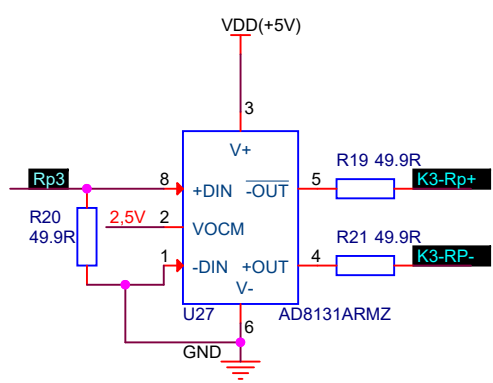
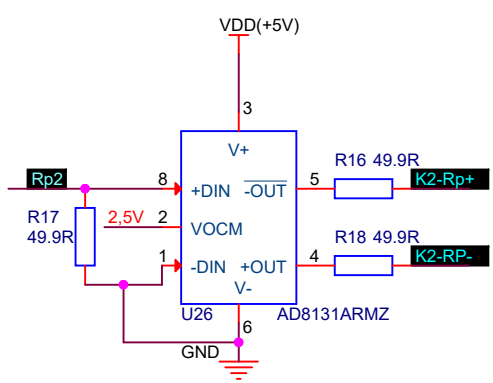
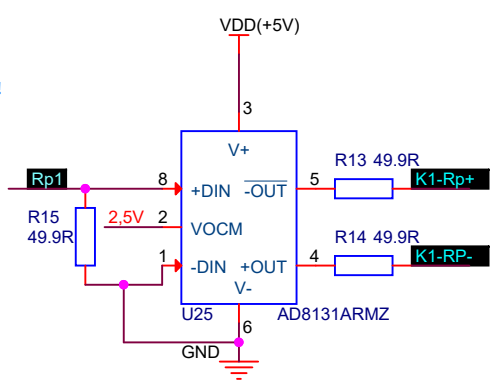
VDD(+5V)



VEE(+3.3V)



5 V TTL-Pegel
wird als gepuffert
f. 50 Ohm angenommen!



Aus max. 8 möglichen Rahmenpulsen
der Timingbereiche
werden 8 ausgewählte pro ADC/Modul
auf die ADC-Eingänge gestellt (100 Ohm diff.)!



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MDR-IO

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